

## Combining the CLC and NCO to Implement a High-Resolution PWM

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### INTRODUCTION

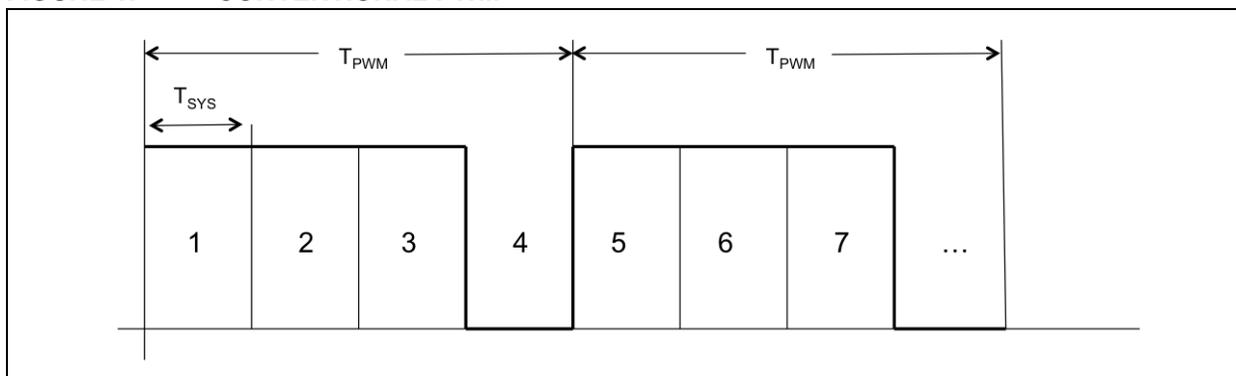
Although many applications can function with PWM resolutions of less than eight bits, there is a range of applications, such as dimming of lamps, where higher resolution is required due to the sensitivity of the human eye.

### BACKGROUND

A conventional PWM uses a timer to produce a regular switching frequency ( $T_{PWM}$ ), and then uses a ripple counter to determine how many clocks the output is held high before the pulse ends.

The output pulse width is adjusted as indicated in [Figure 1](#) to produce, in this case, a PWM with five possible duty cycle settings (0%, 25%, 50%, 75% or 100%).

**FIGURE 1: CONVENTIONAL PWM**



The effective resolution (measured in bits) of a PWM can be calculated by taking the base-2 logarithm of the number of pulse width settings ( $N$ ) possible.

#### EQUATION 1: PWM RESOLUTION

$$Resolution = \log_2(N)$$

For a device running at 16 MHz, the smallest duty cycle adjustment increment would be 62.5 ns (one system clock). If the PWM is configured to run at a switching frequency of 200 kHz (switching period of 5  $\mu$ s), 100% duty cycle will be achieved when the duty cycle register is set to 80 clocks (80 x 62.5 ns = 5  $\mu$ s). This would make the effective PWM resolution only slightly more than six bits, as there are 80 steps to choose from. This is because one system clock divides into one period 80 times.

Knowing that there are 80 possible duty cycle steps, a precise value for the resolution of the PWM can be calculated as follows ([Equation 2](#)):

#### EQUATION 2: PWM RESOLUTION EXAMPLE

$$\log_2 80 = 6.32 \text{ bits}$$

A PWM running from a 16 MHz clock, which has a 10-bit duty cycle register, will start losing resolution due to this limitation at a 15.6 kHz switching frequency. For higher PWM switching frequencies, the duty cycle will reach 100% before all of the steps in the 10-bit duty cycle register have been used, and for all the remaining values the output will simply remain at 100% duty cycle.

The frequency at which this point is reached can be calculated as follows ([Equation 3](#)):

#### EQUATION 3: SWITCHING FREQUENCY LIMITATION

$$\frac{F_{osc}}{\#Steps} = \frac{16MHz}{2^{10}} = \frac{16,000,000}{1024} = 15.6 \text{ kHz}$$

In most PWM applications, the PWM is switched at a much higher frequency than the output can ever change. By filtering this PWM signal using a low-pass filter, the desired output is obtained. The filter removes the high-frequency switching components of the PWM by essentially calculating the average value of the PWM signal, and presents this as the output. For example, in a switching power supply, the output voltage will be directly proportional to the duty cycle. The consequence of this relationship is that the smaller the adjustment to the PWM duty cycle, the smaller the resulting change to the output will be resulting in more precise control of the output.

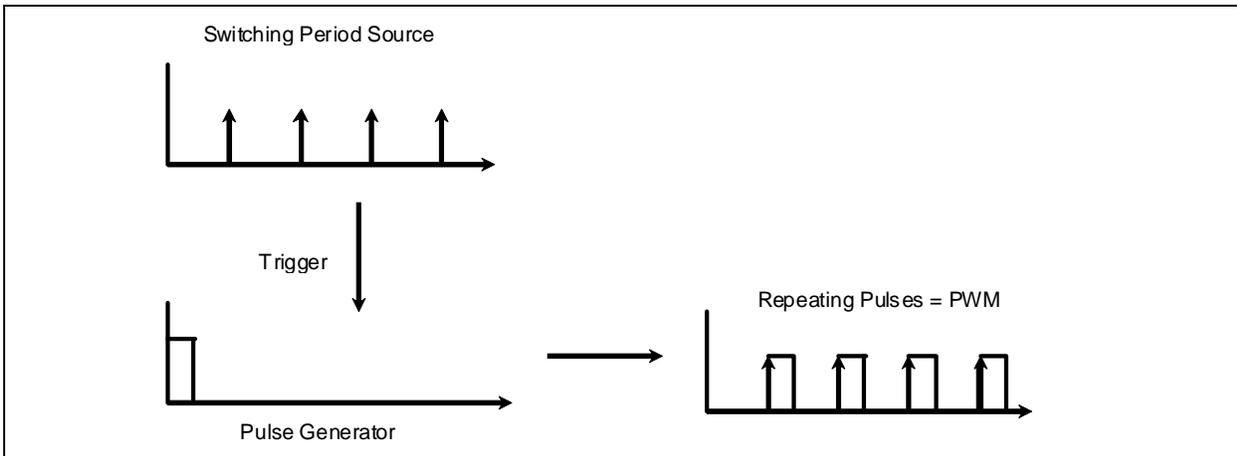
From a control systems point of view, being able to make small adjustments to the output effectively lowers the quantization gain introduced by the PWM. In control systems, this lowering of the gain is important to ensure stability of the system.

## DESIGN

### PWM Construction

In principal, a PWM is created by the combination of the two parameters. The first being a repeating trigger, which determines how often the switching period or switching frequency are pulsed, and the second being a single-pulse generator, which determines how wide the pulse is (the duty cycle). This is illustrated in [Figure 2](#).

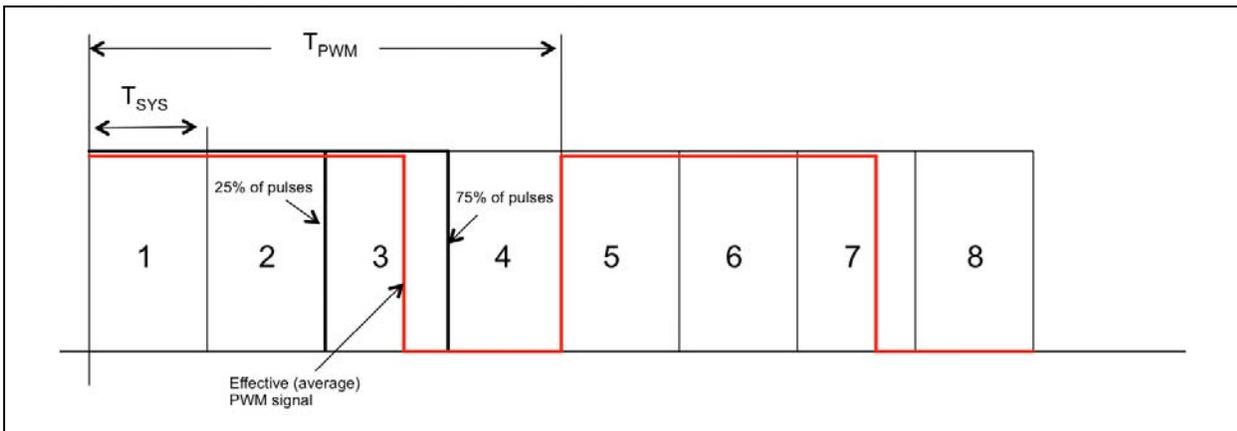
**FIGURE 2: PWM CONSTRUCTION**



In order to achieve an increase in the effective PWM resolution, the NCO peripheral on the PIC<sup>®</sup> device will be used to create a monostable circuit (a circuit that gives a single pulse of fixed duration when triggered).

The NCO will generate a signal that varies between two values in a defined proportion, creating an average pulse width, which is somewhere in between two system clocks, as illustrated in [Figure 3](#). The PWM signal pulse width will vary (jitter/dither) by one clock period, with the proportion/ratio of the variation precisely determined by the NCO configuration.

**FIGURE 3: NCO BASED PWM OPERATION**

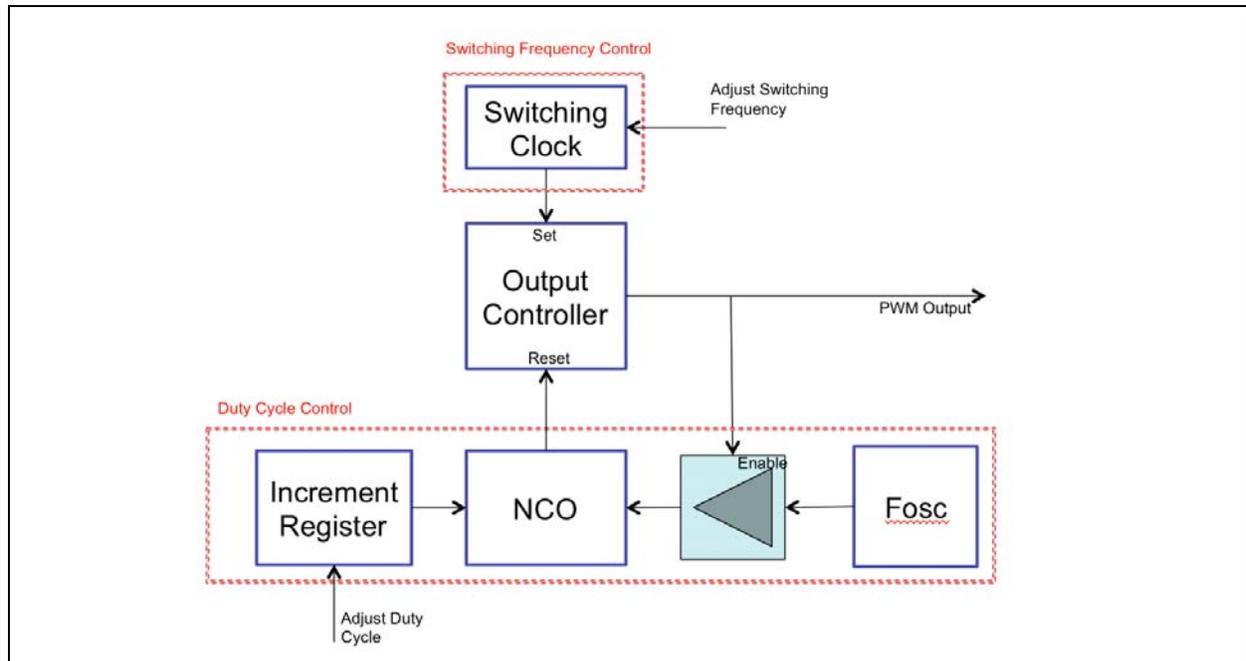


In any application where the output is producing an average value (e.g., average power transfer to the load in SMPS or lighting applications), the variation in pulse width will be perfectly acceptable, because the average pulse width is accurately controlled.

By itself, the NCO peripheral cannot produce a PWM signal, but its behavior can be changed by adding some logic using the CLC to produce a PWM output.

This can be achieved by using the conventional PWM as a clock source to trigger the PWM period, and use the NCO to determine the pulse width. Any number of clock sources could be used (e.g., Timers or even external signals), and in some applications an external trigger can be used to start the pulses, such as a zero-current detection circuit for power supplies. A simplified block diagram of how this will work is shown in [Figure 4](#).

**FIGURE 4: NCO-BASED PWM PRINCIPLE OF OPERATION**



The control logic in the CLC is used to set an output when the switching clock indicates that it is time for the next pulse, and clear this output to complete the pulse once the NCO overflows.

## IMPLEMENTATION USING CLC AND NCO

An implementation of this design using the NCO and CLC is shown in [Figure 5](#). For this design, the NCO is placed in Pulse Frequency mode. In this mode of operation, a short pulse is produced when the NCO overflows.

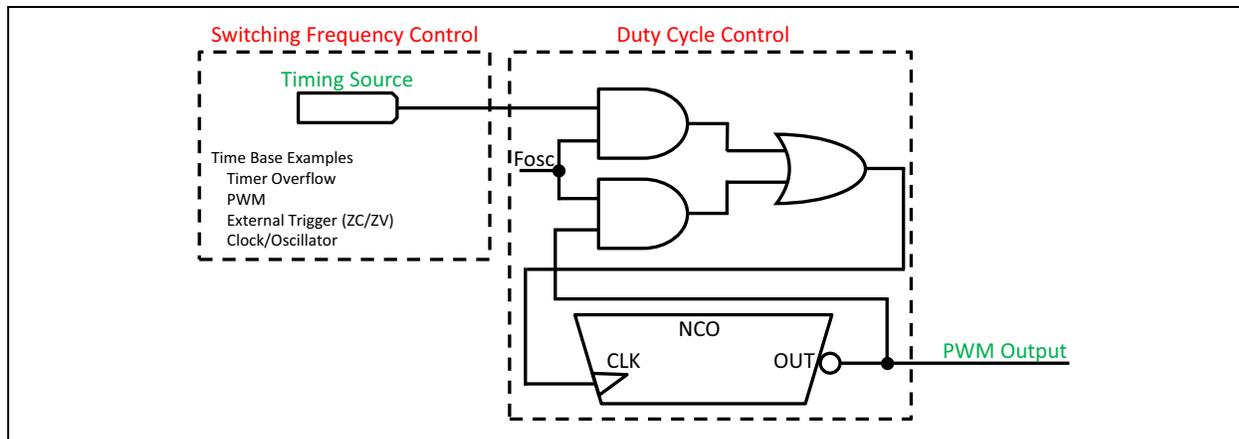
The operation of the circuit can be described as follows:

1. When the system begins, the NCO output is low because it is waiting for enough clocks to count until it overflows and produces a pulse. This low output signal is inverted so that the PWM output becomes high and is fed into U2. This will supply a high-speed clock back into the NCO clock pin via U3.
2. The PWM output will remain high until the accumulator overflows and the NCO output changes. This will cause U2 to stop producing the clock needed to run the NCO. At this point, the NCO is stuck high until it can get the clocks

needed to finish its pulse. The PWM output is now low.

3. The timing source will then pulse high through U1 when the next period begins, feeding the high-speed clock back to the NCO via U3.
4. The NCO uses these few clocks to finish the pulse, and then the output toggles back to the low position where it starts the process over from step 1 above. The amount of time it takes the NCO to overflow will depend on the remainder left in the accumulator after the last overflow, as well as the increment register. Due to the accumulation of remainders the pulse will sometimes be one system clock shorter than usual. By controlling how often this happens (setting the increment register), the exact average pulse width can be controlled.

**FIGURE 5: PWM IMPLEMENTATION USING CLC AND NCO**



## CALCULATIONS

The calculation of the pulse width will be according to the NCO overflow frequency calculation, as listed in the data sheet.

### EQUATION 4: OUTPUT FREQUENCY

$$F_{OUT} = F_{NCO} \times \frac{Increment}{2^n}$$

The average overflow frequency of the NCO will determine the average output pulse width ( $T_{PULSE}$ ) produced.

### EQUATION 5: AVERAGE PULSE WIDTH

$$T_{PULSE} = \frac{1}{F_{OUT}}$$

[Table 1](#) below shows the pulse width, which this circuit will produce using a 16 MHz clock connected directly to the NCO clock input ( $F_{NCO}$ ), given various increment register values. Note that, for high increment values, a single increment of the register will change the pulse width by a mere 15 ps.

**TABLE 1: CALCULATED PWM PULSE WIDTH FOR DIFFERENT INCREMENT REGISTER VALUES**

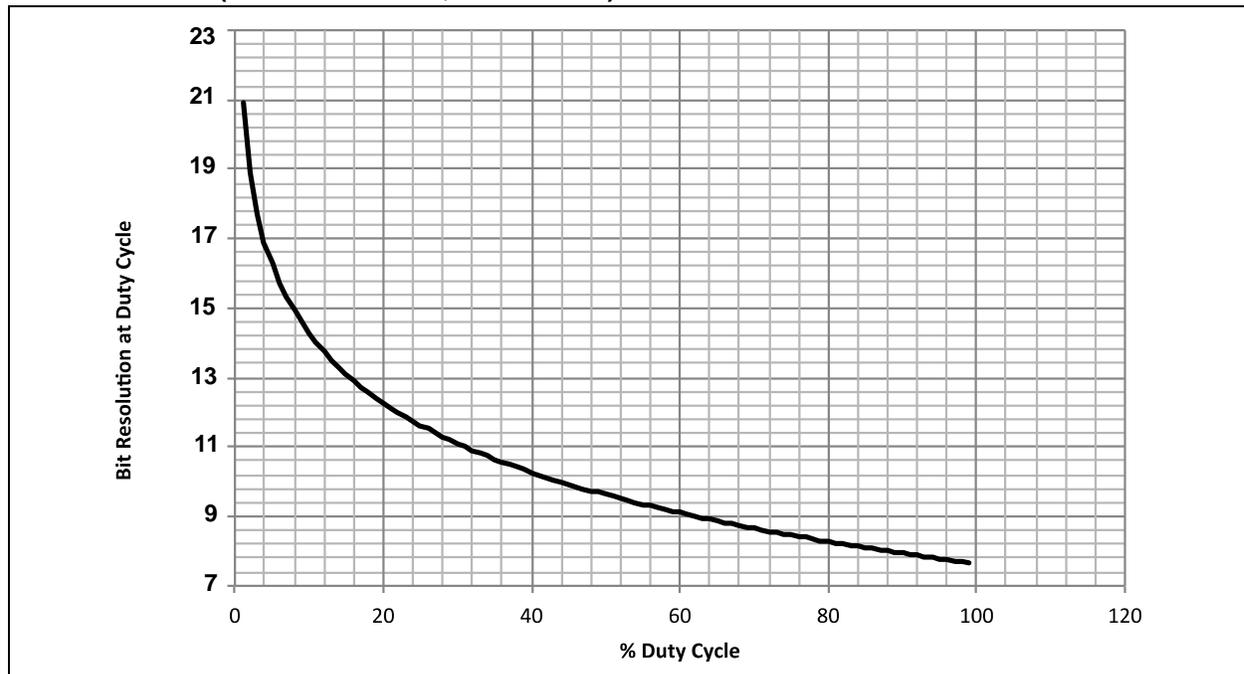
Increment Value	NCO Fout (Hz)	Average Pulse Width (ns)
65000	991,821	1,008.246
65001	991,837	1,008.231
20000	305,176	3,276.800
20001	305,191	3,276.636
100	1,526	655,360.000
101	1,541	648,871.287

## CHARACTERISTICS

It is important to note that the NCO is designed to give linear control over frequency. The control over pulse width is subsequently not linear. As can be seen from the equation for calculating  $T_{PULSE}$  above (Equation 5), the pulse width will vary with the inverse of the frequency ( $1/x$ ).

The result is that the effective resolution of the PWM is not constant over the entire range from 0% to 100% duty cycle.

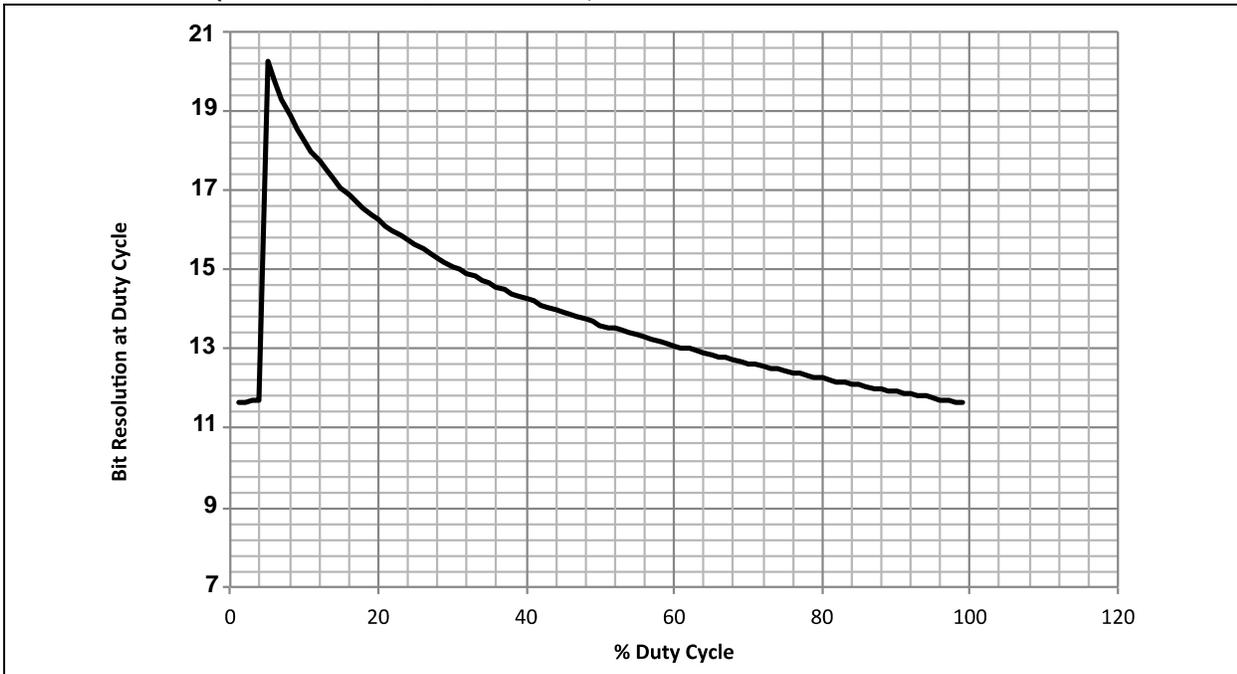
For every duty cycle setting, the effective resolution at this particular point can be calculated and then plotted on a graph. This curve will look different depending on what the switching frequency is, the pulse width being adjusted independently from the switching frequency. For a  $F_{sw} = 3$  kHz and a 16 MHz clock, the graphic will look as follows (Figure 6).

**FIGURE 6: HIGH RES PWM RESOLUTION PLOTTED AGAINST DUTY CYCLE (CLOCK = 16 MHz, Fsw = 3 kHz)**

Although there is an equivalent of 21 bits of resolution close to 0% duty cycle, this deteriorates to only 7.5 bits of resolution at 100% duty cycle, at which point the conventional PWM would outperform our high-resolution implementation.

Interestingly, and perhaps counter-intuitively, the resolution can be improved by decreasing the NCO input clock frequency. Reducing this clock to 1 MHz will have the result shown below (Figure 7).

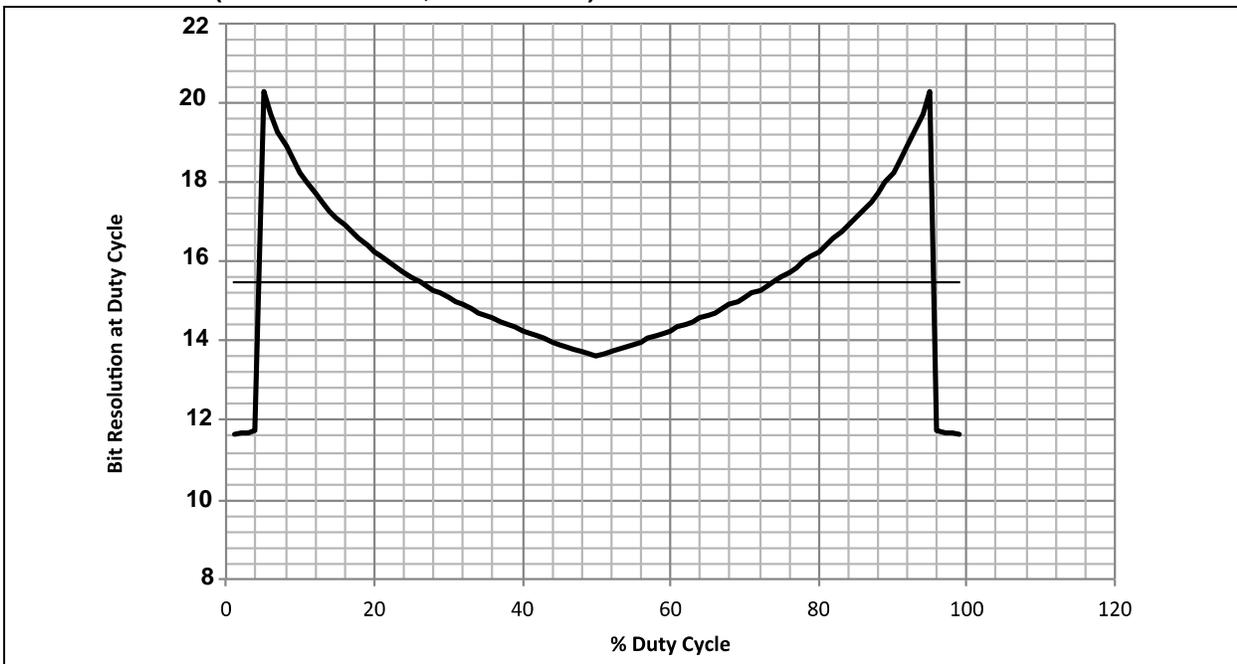
**FIGURE 7: HIGH RES PWM RESOLUTION PLOTTED AGAINST DUTY CYCLE (CLOCK = 1 MHz, Fsw = 3 kHz)**



There is, of course, a limitation, as can be seen, close to 0% duty cycle, where the increment register maximum value is reached and smaller pulses cannot be generated any more, but the resolution now never reduces to less than 11 bits.

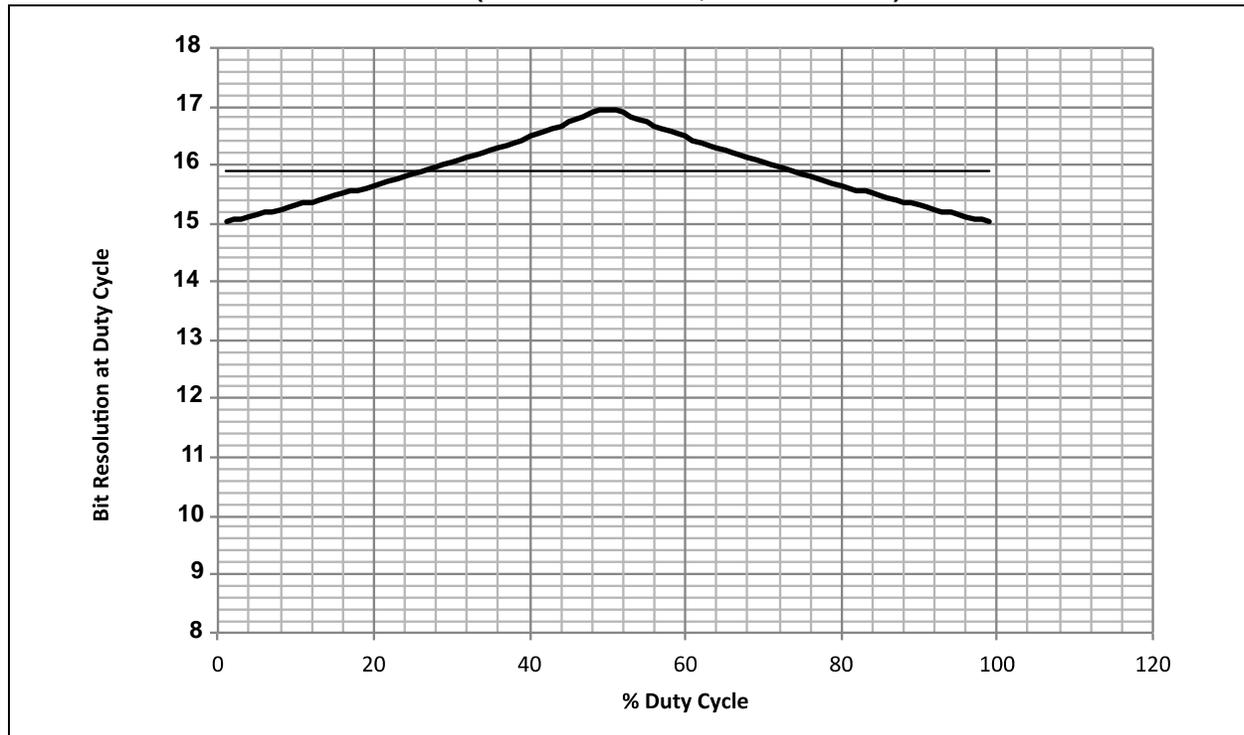
One way to improve the performance would be to invert the PWM signal when it exceeds 50% duty cycle. Doing this can effectively mirror the performance under 50% duty cycle to the region above it, with the higher resolution. There is still the option to use the original curve where the limits of the increment are reached. This results in the following graphic (Figure 8) for the same conditions as the graphic above.

**FIGURE 8: RESOLUTION VS DUTY CYCLE WITH SIGNAL INVERSION AT 50% DUTY CYCLE (CLOCK = 1 MHz, Fsw = 3 kHz)**



When the intention is to achieve both the highest possible switching frequency and the highest resolution using this technique, the configuration shown below can be used (Figure 9). This graphic shows the achievable resolution when using a 16 MHz clock at a switching frequency of 500 kHz.

**FIGURE 9: HIGH RES PWM RESOLUTION PLOTTED AGAINST DUTY CYCLE WITH INVERSION AT 50% (CLOCK = 16 MHz, F<sub>sw</sub> = 500 kHz)**



## SUMMARY

Conventional PWMs start losing effective resolution at relatively low-switching frequencies. For applications where the switching frequencies have to be fairly high, and having as much PWM resolution as possible at these frequencies is necessary, the NCO can be used in conjunction with the CLC to create a very high-resolution PWM output.

The smallest incremental change in pulse width achievable by a conventional PWM with a 16 MHz system clock speed would be 62.5 ns. If the fastest available PWM clock is  $F_{osc}/4$ , then this increases to 250 ns.

On the same device, a PWM with an incremental pulse width change of as little as 15 ps can be constructed using the technique described in this application note.

Even if the requirement is not primarily high resolution, this solution may still be attractive for a number of applications, adding an additional PWM to the capability of the device, or having a constant on/off-time variable frequency PWM, where the pulse is triggered externally as required, when doing zero current switching in high-efficiency power converters.

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