AN2133

Extending PIC® MCU Capabilities Using CLC

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INTRODUCTION

The Configurable Logic Cell (CLC) is a flexible peripheral that enables creation of on-chip custom logic functions for PIC® microcontrollers. This peripheral allows the user to specify combinations of signals as inputs to a logic function, and to use the logic output to control other peripherals and I/O pins. This provides greater flexibility and potential to embedded designs as the CLC operates independently of the CPU in a microcontroller.

The core independent peripherals handle their tasks with no code or supervision from the CPU to maintain their operation. This makes the CLC a peripheral that simplifies the implementation of complex control systems and gives the designers the flexibility to innovate.

Overview of CLC

The CLC is a user-configurable peripheral, similar to a Programmable Logic Device (PLD). Various internal and external inputs can be chosen as inputs to the CLC. The CLC receives inputs from other peripherals or from an input pin. It then performs the intended logic operation and provides an output that can be used to control other peripherals or another I/O pin.

A brief insight into the four stages of the CLC peripheral is as follows:

- Input Selection

  The CLC can receive a number of signals, such as internal clocks, output of another peripheral, and events of peripherals, such as a timer input.

- Signal Gating

  The selected input signal sources can be directed to the desired logic function through the signal gating stage.

- Logic Function Selection

  In the CLC, the outputs of the data gating stage are inputs to the logic function selection stage. The CLC supports logic functions, such as AND-OR, OR-XOR, AND, SR latch and D-Flip Flops (D-FF).

- Output Polarity Selection

  The output polarity stage is the last stage in the CLC. The desired polarity of the logic output can be selected.

Refer to "**Configurable Logic Cell (CLC)"** (DS33949) in the *"dsPIC33/PIC24 Family Reference Manual"* or the specific device data sheet for more information on the input sources, signal gating and logic functions available in the CLC.

Benefits

Some of the CLC usage examples are as follows:

- The CLC can be used as a stand-alone peripheral in implementing sequential and combinational logic functions, thus facilitating quick event triggers and responses.
- The CLC, used in conjunction with other peripherals, helps in extending the capabilities of that peripheral by facilitating custom complex functionality implementation in the hardware.
- The CLC being a core independent peripheral effectively reduces the CPU bandwidth requirement for an application, as many simple logic and event responses can be offloaded from the CPU to the peripheral.
- The CLC reduces Flash and RAM requirements as the software algorithms are not required.
- The logic functions implemented in the hardware have faster event response when compared to the logic functions implemented in the software.
- The CLC supports a higher level of integration without any external components and reduced PCB size.

Applications of CLC

The versatile features of the CLC, along with its simplicity, helps in extending the capabilities of a PIC® MCU device. The following are a few applications of the CLC that are discussed in this document:

- Application 1: Phase Detector
- Application 2: Complementary Waveform Generator with Dead-Band Control of SCCP
- Application 3: Data Signal Modulator (DSM) without Synchronization
- Application 4: Multiple Parameter Monitoring
- Application 5: NRZ to RZ Encoding
- Application 6: 2x1 Multiplexer

APPLICATION 1: PHASE DETECTOR

Measuring phase angle between two signals of the same frequency is useful in a wide range of applications, including metering, digital power systems, communication and medical instruments.

The CLC can be used to measure the phase difference between two signals of the same frequency. The AND-OR logic function in the CLC can be used to implement an XOR function to measure the magnitude of phase difference and the D-FF logic function helps in obtaining lead/lag information of the signals.

Note:	Besides square waves, it is possible to measure the phase between other types of analog signals, such as sinusoidal waves.

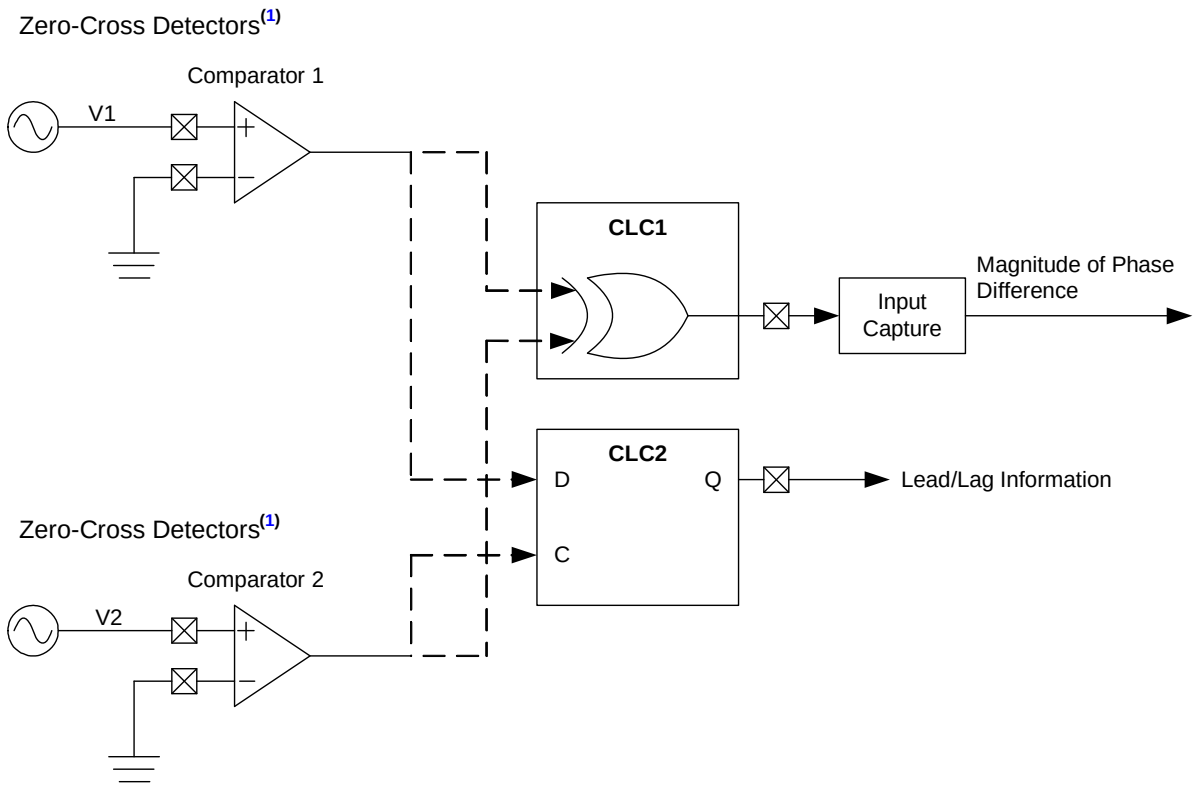
Implementing a phase detector, using the CLC, provides an increased system flexibility when the output of a comparator is internally routed to the CLC.

Figure 1 depicts the configuration of CLC as a phase detector.

The peripherals required for this application are:

- Comparator 1 and Comparator 2 as Zero-Cross Detectors (ZCDs)
- CLC1 and CLC2
- Input Capture (IC)

FIGURE 1: PHASE DETECTOR(2)



Note 1: Comparator pins require a safety circuit when interfacing with an AC line. The circuit needs current-limiting resistors and voltage limiting Schottky diodes.

2: Dashed lines shown in the figure represent internal connections.

ZCD to Convert Analog Signals to Square Waves

The source signals whose phase difference are to be measured are fed as inputs to two comparators, which are configured as ZCDs to convert the input analog signals into square waves of the same frequency. If source signals are known to be square waves, then the ZCDs are not required and the source signals can be directly fed to the CLC input pins (CLCINA and CLCINB). If a ZCD is required, then the generated square waves are internally routed as inputs to the CLC modules.

CLC1 and IC to Determine Magnitude of Phase Difference

CLC1 and the IC are used for determining the magnitude of phase difference. CLC1 is configured in AND-OR logic function from which XOR functionality is derived. The XORed output of CLC1 is externally connected as the source signal to the IC. The pulse width of the XORed output gives the magnitude of phase difference between the two waves and is measured by the IC. On every edge of the CLC1 output, the IC generates an interrupt with its internal timer (ICTMR) value stored in the buffer, and then the buffer values can be read in software. If the CLC1 output produces no signal, then source signals are in phase. Figure 2 shows the timing diagram for various phase difference scenarios.

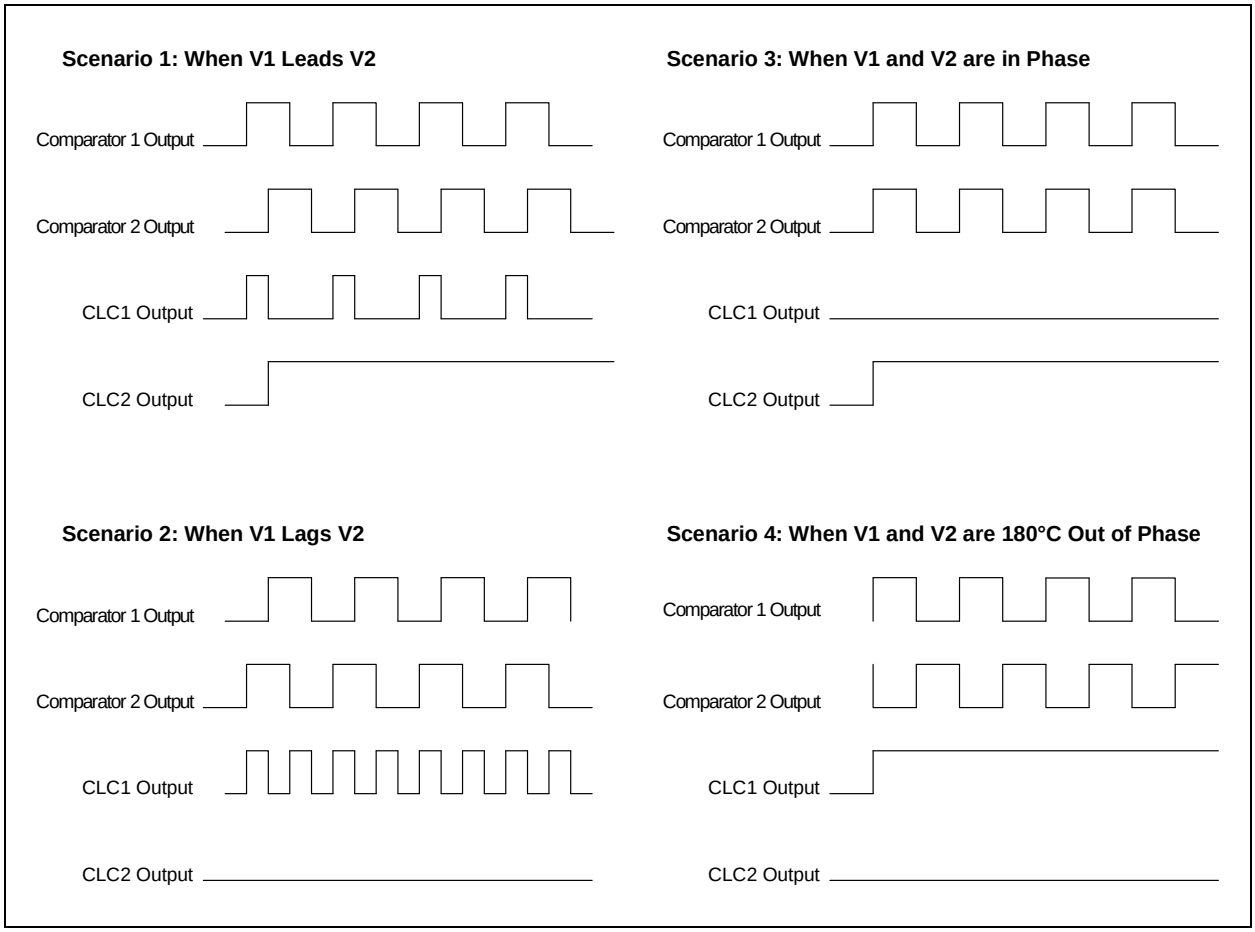
CLC2 to Determine Lead/Lag Information

The square waves generated from the ZCDs are fed to CLC2 to determine the lead/lag information.

CLC2 is configured in 1-Input D-FF mode by using two ZCD output signals; one used as the D input and the other as the clock of D-FF. The output of CLC2 gives the phase lead/lag information, as shown in Figure 2.

Note:	The maximum and minimum frequency that can be measured using the IC depends on the processor speed relative to the input signal frequency. Refer to the device data sheet for more information on the maximum/minimum signal frequency that can be measured by using an IC.

FIGURE 2: TIMING DIAGRAM OF PHASE DETECTOR



Usage Examples

Applications of a phase detector using the CLC are discussed in the following sections.

USAGE EXAMPLE 1: DISTANCE MEASUREMENT

A phase detector can be used for distance measurements. The continuous wave of the RF is transmitted towards a target. The distance to the target is proportional to the phase shift between the transmitted and received waves. The transmitted and received waves are used as inputs to the CLC, and the phase difference between the two signals at the CLC output can be used for calculating the distance between the source and target. Figure 3 shows the use of the CLC in distance measurement, and Figure 4 shows transmitted and reflected waves. Distance as function of the phase shift is given by Equation 1:

EQUATION 1:

$$d = \frac{\phi\lambda}{4\Pi} = \frac{\phi c}{4\Pi f}$$

Where:

d = distance of the unknown object

ϕ = phase difference between the transmitted and reflected waves

λ = wavelength of the transmitted wave

f = frequency of the transmitted wave

c = velocity of the transmitted wave

FIGURE 3: DISTANCE MEASUREMENT BASED ON PHASE DIFFERENCE CALCULATION

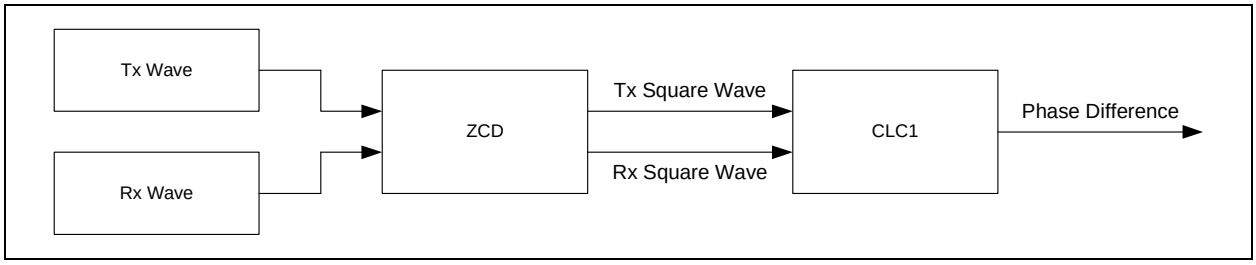
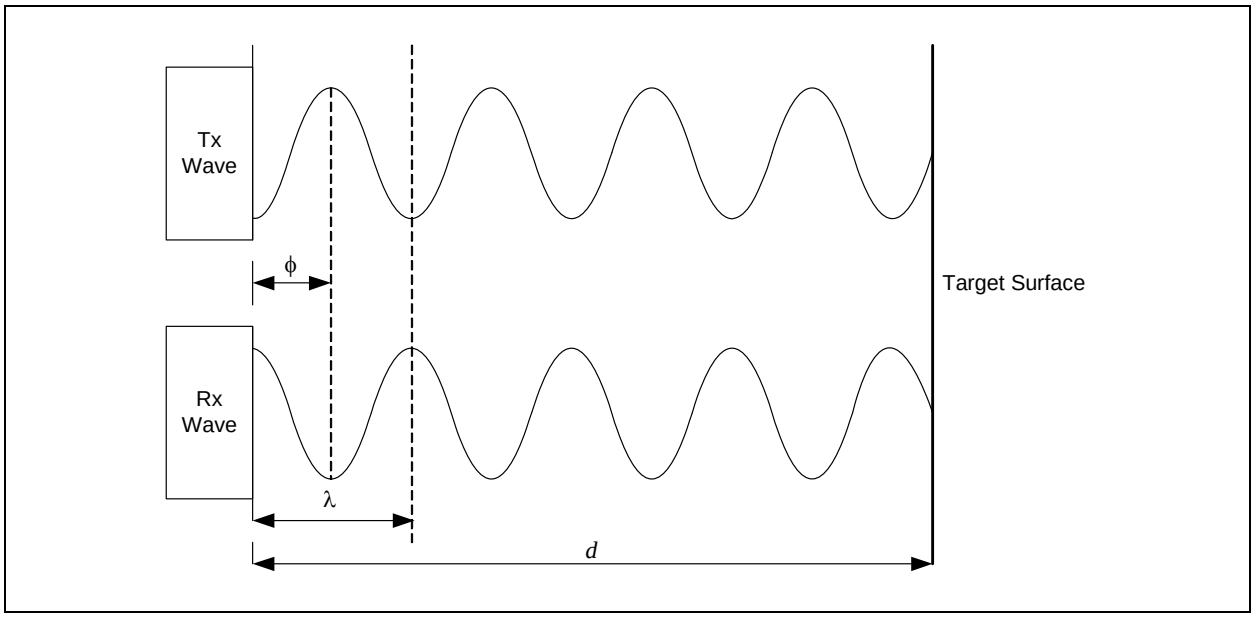


FIGURE 4: TRANSMITTED AND RECEIVED WAVES



USAGE EXAMPLE 2: ENERGY MEASUREMENT

Instantaneous electric power in an AC circuit is given by the equation: $P = VI$, but these quantities are continuously varying. The desired power in an AC circuit is the average power and is due to its resistive component. It is given by Equation 2:

EQUATION 2:

$$P_{avg} = VI\cos\varphi$$

Where:

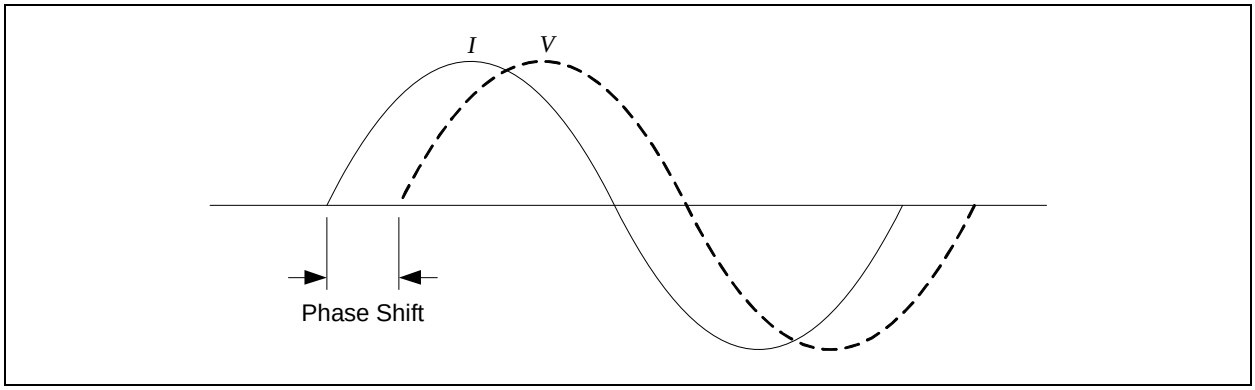
φ = phase angle between current and voltage

VI = rms values of voltage and current, respectively

$\cos\varphi$ = "power factor" which helps calculate active and reactive power components

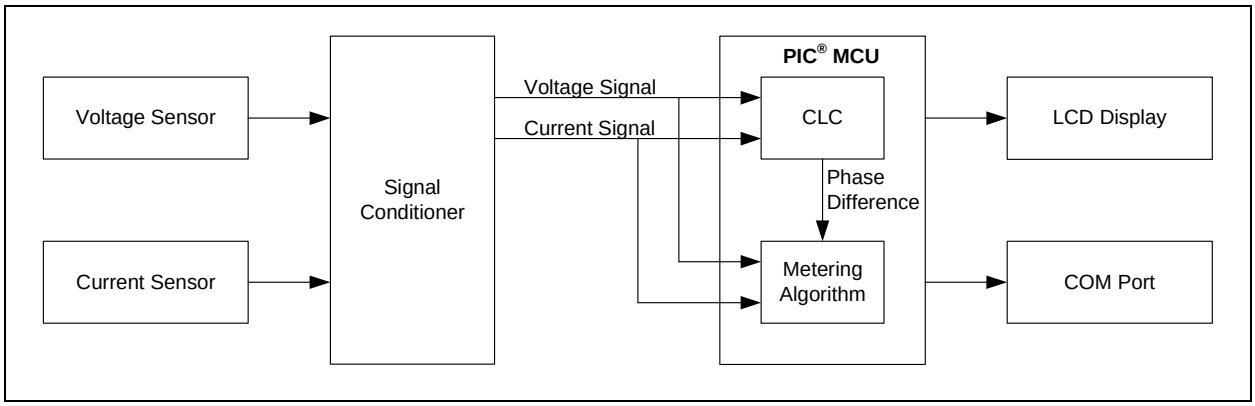
Since measurement of phase difference between V and I is involved in the calculation of average power, the CLC module can be used for this purpose. This principle of energy measurement can be used in a digital energy meter. Figure 5 shows the phase shift between current and voltage.

FIGURE 5: PHASE SHIFT BETWEEN CURRENT AND VOLTAGE



The components of a digital meter are shown in Figure 6. The voltage and current sensor outputs are fed to a signal conditioner, which ensures a matched signal level to the control circuit. The conditioned signals are then fed to a phase detector using the CLC, as illustrated in Figure 1. The current, voltage and cosine of the determined phase are multiplied to obtain the power consumed by the load. The lead/lag information can be used to determine whether the load is inductive or capacitive.

FIGURE 6: BLOCK DIAGRAM OF DIGITAL ENERGY METER



APPLICATION 2: COMPLEMENTARY WAVEFORM GENERATOR WITH DEAD-BAND CONTROL OF SCCP

The Complementary Waveform Generator (CWG) produces a complementary waveform with a dead-band control from its input source. A dead-band time is inserted between two signals to prevent shoot-through current in various power supply applications.

This application illustrates the use of the CLC peripheral's edge detection and interrupt capabilities in generating a complementary waveform with a Single Capture/Compare/PWM (SCCP) module as its input source.

Often, applications, such as motor control, require several complementary waveform generators to control their functioning. The Multiple Capture/Compare/PWM (MCCP) module is capable of producing complementary waveforms with non-overlapping signals by controlling the dead band at its output. However, if the application requires more instances of MCCP than what is available in the device, then the SCCP could be used. The CLC peripheral, in conjunction with the SCCP, can be used to generate a complementary waveform with the required dead band, as the SCCP on its own cannot generate non-overlapping signals.

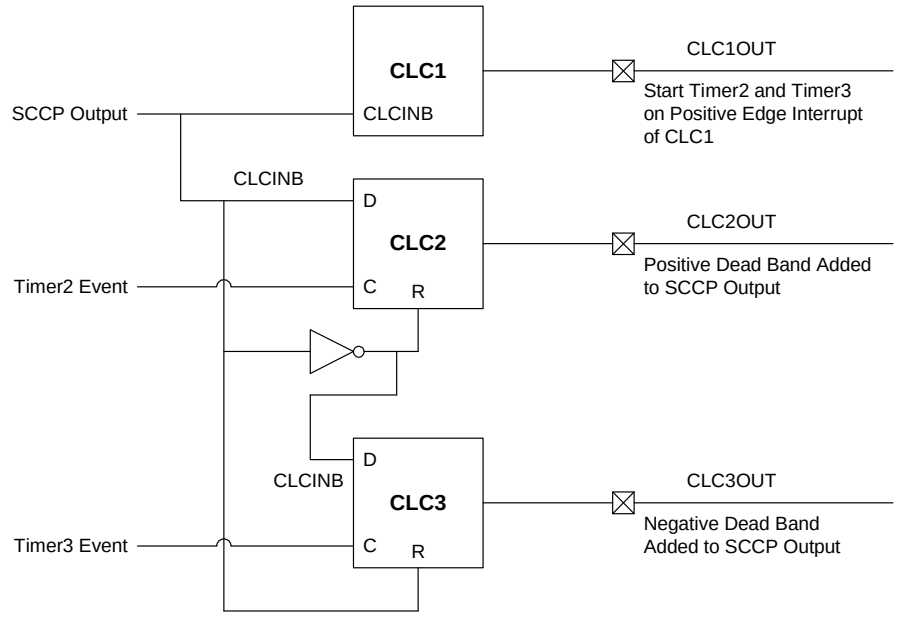
Modes of Operation

A dead band can be added for both edge-aligned and center-aligned SCCP outputs. These configurations are described in the following sections.

EDGE-ALIGNED MODE

Figure 7 shows the configuration of CLC1, CLC2 and CLC3 to control the dead band of the SCCP output in an Edge-Aligned mode.

FIGURE 7: CWG IN EDGE-ALIGNED MODE USING CLC



Note: Inverter operation shown in the figure is done using the CLC register bits.

The peripherals required for this application are:

- CLC1, CLC2, CLC3
- Timer2
- Timer3

Configuring SCCP: Configure the SCCP peripheral to generate an edge-aligned PWM output. If the SCCP is available as one of the input sources, then CLC1, CLC2 and CLC3 are configured to use it as an input source. Else, the SCCP output has to be externally connected to the CLCINB pin. For more information, refer to the specific device data sheet.

Configuring Timer2 and Timer3: Timer2 is configured to add a rising edge dead-band delay, whereas Timer3 is configured to a add A falling edge dead-band delay.

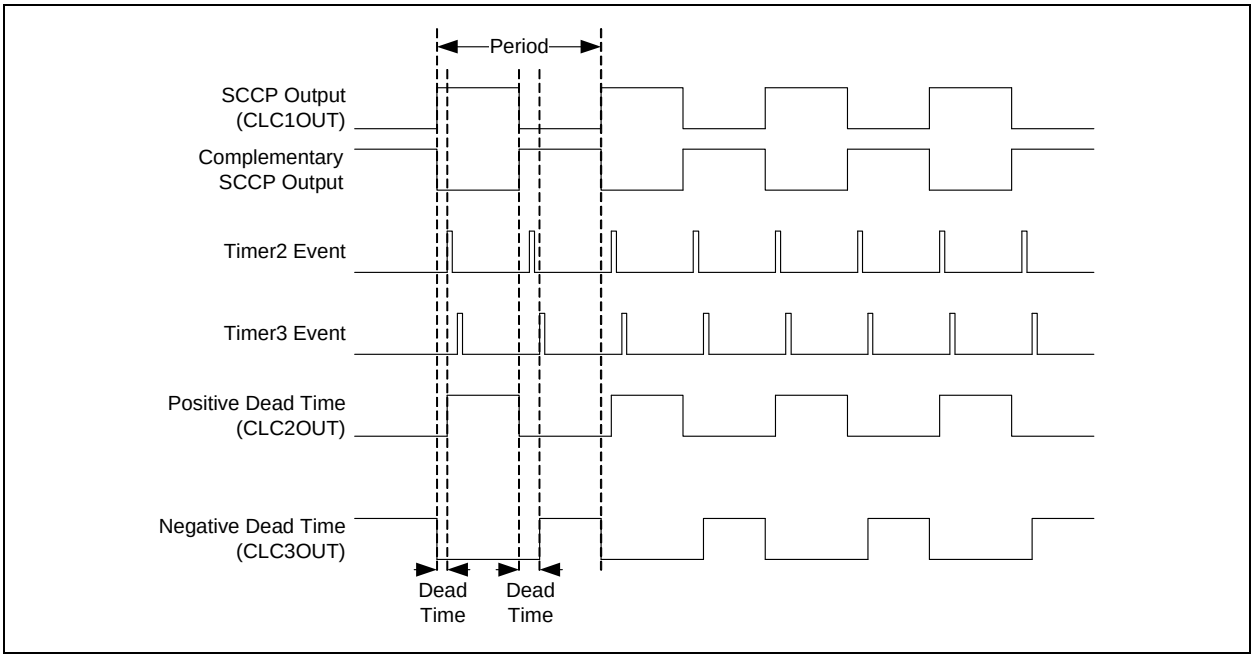
Configuring CLC1 as a Rising Edge Detector: CLC1 is configured in AND mode. On detecting a rising edge of the SCCP output, CLC1 generates an interrupt. On a CLC1 interrupt, Timer2 and Timer3 are turned on.

Configuring CLC2 to Add a Rising Edge Dead Band: CLC2 is configured in 1-input D-FF mode. The SCCP output is used as the data input and its complement as the Reset signal, while the Timer2 event acts as a clock source for the D-FF. CLC2OUT gives the SCCP output with the dead band added to the rising edge. Figure 8 shows signals from different peripherals for generating CLC2OUT.

Configuring CLC3 to Add a Falling Edge Dead Band: CLC3 is configured in 1-input D-FF mode. The SCCP output is used as the Reset signal and its complement as the data input, while the Timer3 event acts as a clock source for the D-FF. The generated output is routed through CLC3OUT. Thus, CLC3OUT gives the SCCP output with the dead band added to the falling edge.

Figure 8 shows signals from different peripherals for generating CLC3OUT.

FIGURE 8: DIFFERENT SIGNALS OF CWG IN EDGE-ALIGNED MODE USING CLC



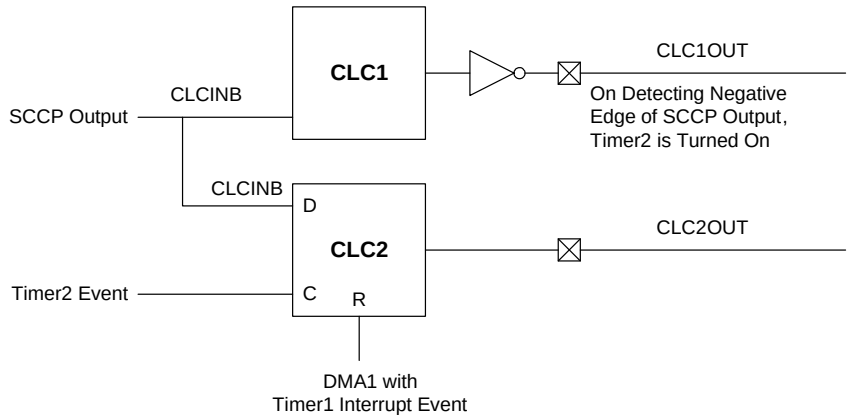
CENTER-ALIGNED MODE

Figure 9 shows the configuration of CLC1 and CLC2 to control the dead band of the SCCP output.

The peripherals required for this application are:

- CLC1 and CLC2
- Timer2
- DMA1

FIGURE 9: CWG IN CENTER-ALIGNED MODE USING CLC



Note: Inverter operation shown in the figure is done using the CLC register bits.

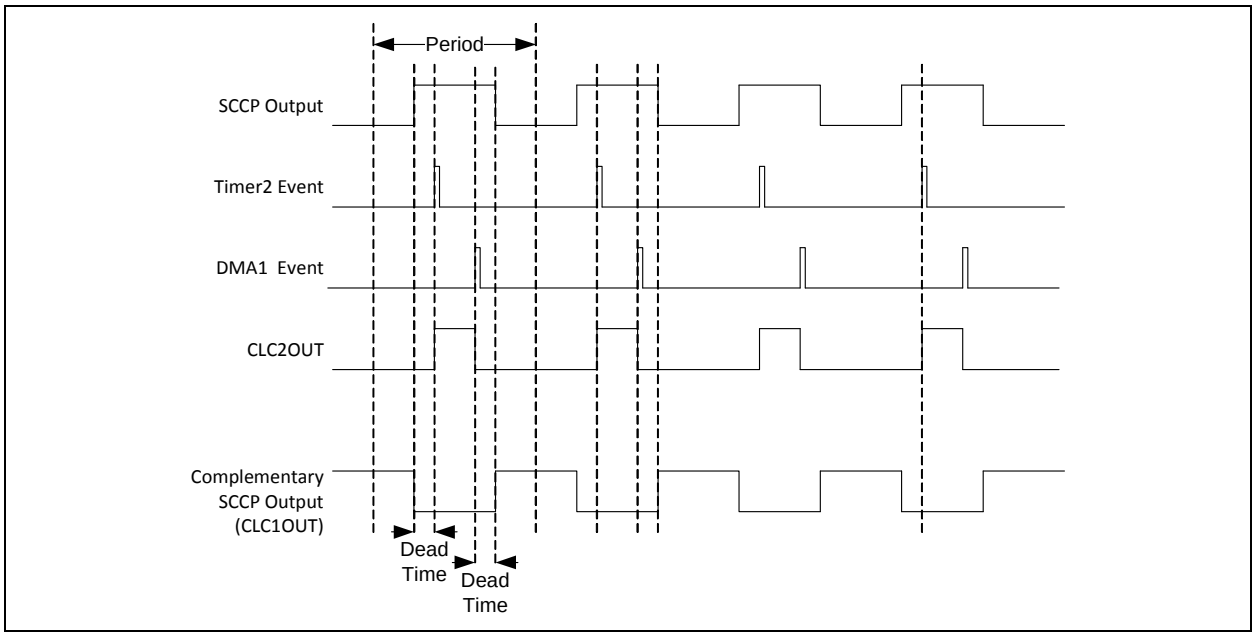
Configuring SCCP: Configure the SCCP peripheral to generate a center-aligned PWM output. If the SCCP is available as one of the input sources, then CLC1 and CLC2 are configured to use it as an input source. Else, the SCCP output has to be externally connected to the CLCINB pin. For more information, refer to the specific device data sheet.

Configuring Timer1, Timer2 and DMA1: Timer2 is configured for the required dead-band delay after the falling edge of the CLC1 output. Timer1 is configured for the required pulse width to be produced. Timer1 is used as a trigger source for DMA1. When Timer1 matches with PR1, DMA1 generates an interrupt event which is used as the Reset signal for CLC2.

Configuring CLC1 as a Falling Edge Detector: CLC1 is configured in AND mode with its output complemented. On detecting a falling edge at its output, CLC1 generates an interrupt. On detecting the CLC1 interrupt, Timer2 is turned on. When Timer2 generates an interrupt, Timer1 is turned on.

Configuring CLC2 to Add a Dead-Band Delay: CLC2 is configured in D-FF mode. The SCCP output is used as a data input, with a Timer2 event as the clock input, and DMA1 with a Timer1 interrupt event as the Reset signal. The output of CLC2 is complementary to the output of CLC1 with a dead-band delay. Figure 10 shows the different signals of CLC for a Center-Aligned mode.

FIGURE 10: DIFFERENT SIGNALS OF CWG IN CENTER-ALIGNED MODE USING CLC

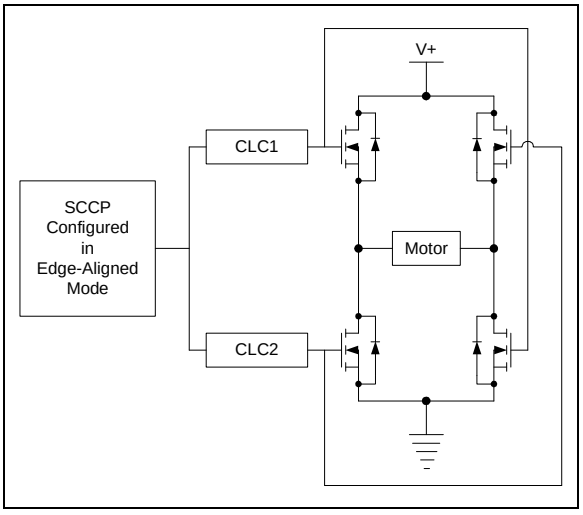


Usage Example: Full-Bridge Motor Control Using CLC

A full-bridge motor driver circuit can be driven by using an MCCP peripheral with its output producing a complementary waveform. However, if several such full-bridge motor driver circuits are to be driven, and a number of MCCP peripherals available on the device are insufficient, then an SCCP, in combination with the CLC, can be used.

Set up an SCCP peripheral and the CLC with the required dead-band delay, as explained earlier. The CLC output signals will be used to drive the motor driver circuit, thus preventing any shoot-through current. Figure 11 shows the CLC peripherals driving a full-bridge driver circuit.

FIGURE 11: FULL-BRIDGE MOTOR DRIVER USING CLC



APPLICATION 3: DATA SIGNAL MODULATOR (DSM) WITHOUT SYNCHRONIZATION

In telecommunications, modulation is a process of transmitting a message signal inside another signal (known as a carrier signal) that can be physically transmitted. A carrier signal is a waveform that is modulated with an input signal for the purpose of conveying information. This carrier wave is usually of a much higher frequency than the input signal.

The Data Signal Modulator (DSM) allows the user to mix a data stream (modulator signal) with a carrier signal to produce a modulated output. The carrier signal is comprised of two distinct signals: a Carrier High (CARH) signal and a Carrier Low (CARL) signal. During the time in which the Modulator (MOD) signal is in a logic high state, the DSM mixes the CARH with the modulator signal. When the Modulator signal is in a logic low state, the DSM mixes the CARL with the modulator signal. This modulation operation can be performed using the CLC.

The advantages of using the CLC for Data Signal Modulation are:

- Data sources, such as UART and SPI, are available as input sources to the CLC, and hence, external wiring can be avoided to use them as sources.
- Different clock sources, such as the SOSC, LPRC and system clock, are available as input sources to the CLC. These sources can be used to modulate the data.
- The capability of the CLC to get external inputs through CLCINA and CLCINB enables the external modulator signal and the carrier signal to be used in the modulation process.

Description of DSM Using CLC

The peripherals required to implement different modulation techniques are:

- CLC
- Modulator Signal Source Peripherals: Some of the communication data sources available as inputs to the CLC are:
  - UART
  - SPI

Note:	If other communication data sources are required to be modulated, then the CLC input pin, CLCINA, can be used. For more information, refer to the specific device data sheet.

- Carrier Signal Source Peripherals: Some of the available peripherals that can be used as carrier signals are:
  - MCCP output
  - System clock
  - LPRC
  - SOSC

Note:	If other carrier signals are required, then the CLC input pins can be used. For more information, refer to the specific device data sheet.

Configuring the Data Signal to be Modulated: The peripheral whose data is to be modulated is configured as per the required specifications. The output of this peripheral is either internally or externally fed as one of the inputs to the CLC.

Configuring the CLC to Modulate Source Data to be Transmitted: The CLC is configured in AND-OR mode. The data signal to be modulated and the carrier signal source are fed as inputs to the AND gate. Different digital modulation schemes and their implementations are explained in the following section.

Digital Modulation Techniques Supported by DSM

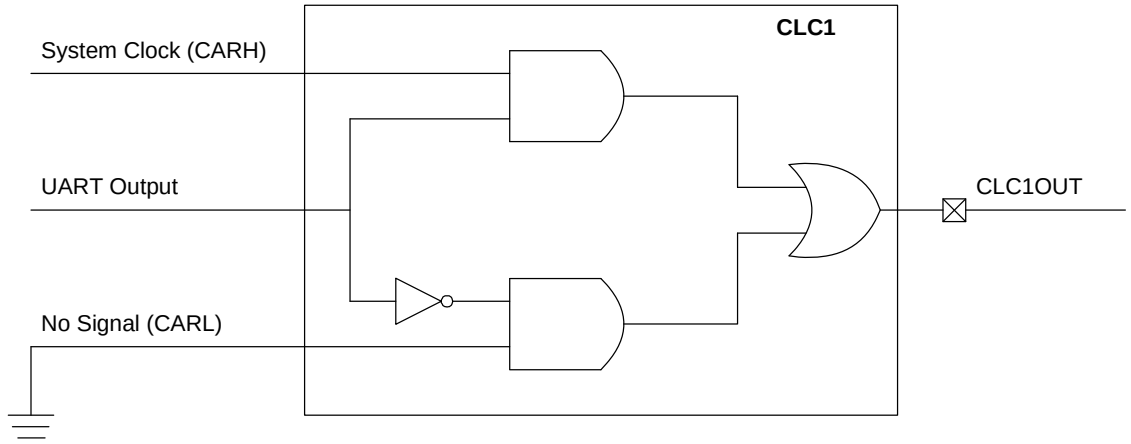
There are three different digital modulation techniques supported by DSM; they are discussed in the following sections:

ON-OFF KEYING (OOK)

In OOK modulation, the logic '1' state of the modulator signal is modulated with the carrier wave, CARH, while logic '0' is represented by the absence of a signal.

Figure 12 depicts the configuration of the CLC to generate OOK.

FIGURE 12: OOK MODULATION IN DSM USING CLC



Note: Inverter operation shown in the figure is done using the CLC register bits.

The peripherals required for this application are:

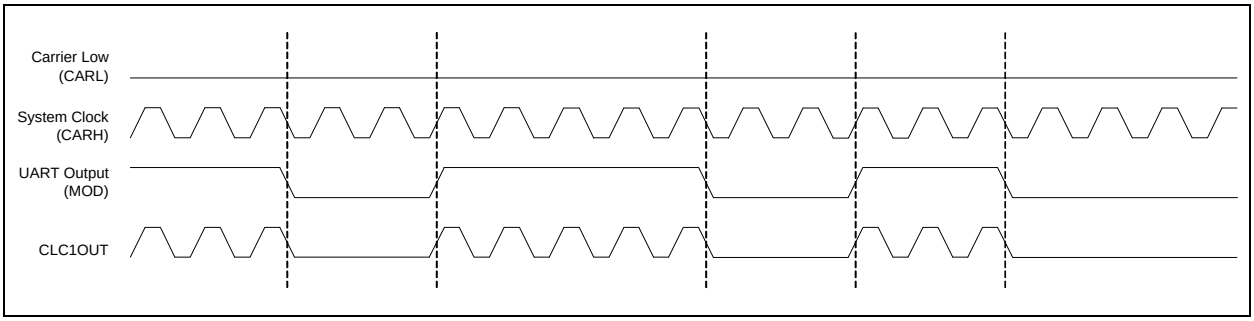
- CLC1
- UART data as the modulator signal
- System clock as the carrier signal

Note: The UART and system clock are used as an example for the modulator signal and carrier signal, respectively. However, it is possible to choose other sources of modulator and carrier signals.

Configuring UART: The UART module is configured to transmit the required data.

Configuring CLC to Modulate UART Transmitted Data: The CLC is configured in AND-OR mode. The system clock is used as the CARH signal to modulate logic '1' and is ANDed with the UART data. Since logic '0' is not modulated, no CARL signal is required. The OOK modulated output of the CLC can be made available on the external pin, CLC1OUT. The CLC1OUT pin is routed to the physical layer of the subsequent communication interface. Figure 13 shows different signals for OOK.

FIGURE 13: OOK USING CLC

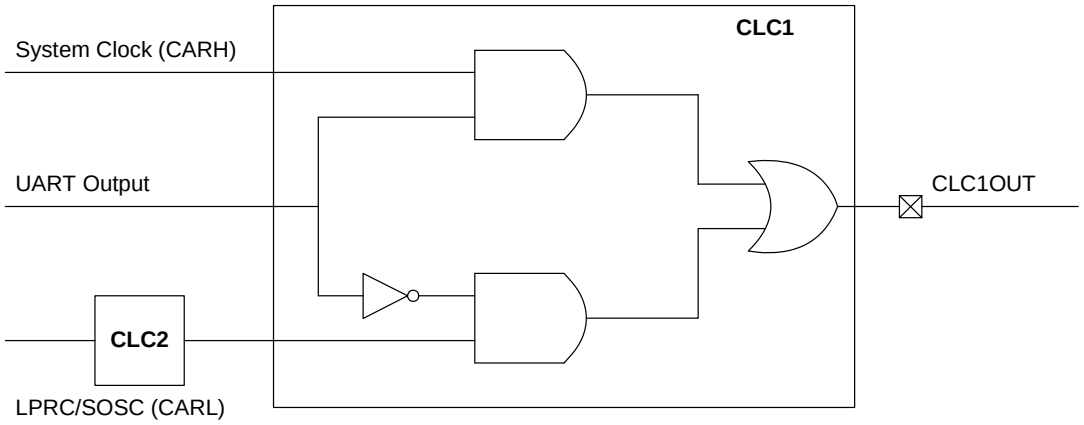


FREQUENCY SHIFT KEYING (FSK)

In FSK modulation, logic '1' is modulated with the high-frequency carrier wave, CARH, while the logic '0' state is modulated with the low-frequency carrier wave, CARL.

Figure 14 depicts the configuration of CLC1 to generate FSK.

FIGURE 14: FSK MODULATION IN DSM USING CLC



Note: Inverter operation shown in the figure is done using the CLC register bits.

The peripherals required for this application are:

- CLC1 and CLC2
- UART data as the modulator signal
- System clock to modulate logic '1'
- LPRC to modulate logic '0'

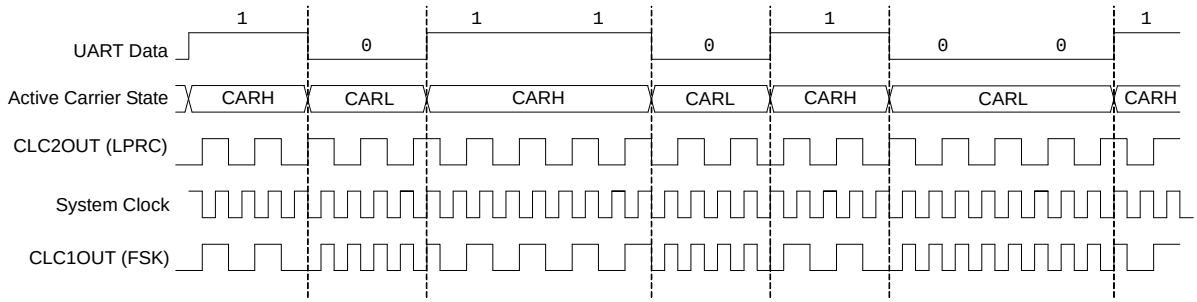
Note:	The UART, system clock and LPRC are used as an example for the modulator signal and carrier signal, respectively. However, it is possible to choose other sources as modulator and carrier signals.

Configuring UART: The UART module is configured to transmit the required data.

Configuring CLC2 to Output LPRC: The CLC2 is configured in AND mode. LPRC is routed through CLC2 and internally fed as an input to CLC1.

Configuring CLC1 to Modulate UART Transmitted Data: CLC1 is configured in AND-OR mode. The system clock is used as the CARH signal to modulate logic '1' and is ANDed with the UART data. The output of CLC2 is used as the CARL signal to modulate logic '0' and is ANDed with the complement of the UART data. Both are combined with an OR gate to produce an output on CLC1OUT, which is the required FSK modulated data. CLC1OUT is routed to the physical layer of the subsequent communication interface. Figure 15 shows different signals for FSK.

FIGURE 15: FSK USING CLC1 AND CLC2

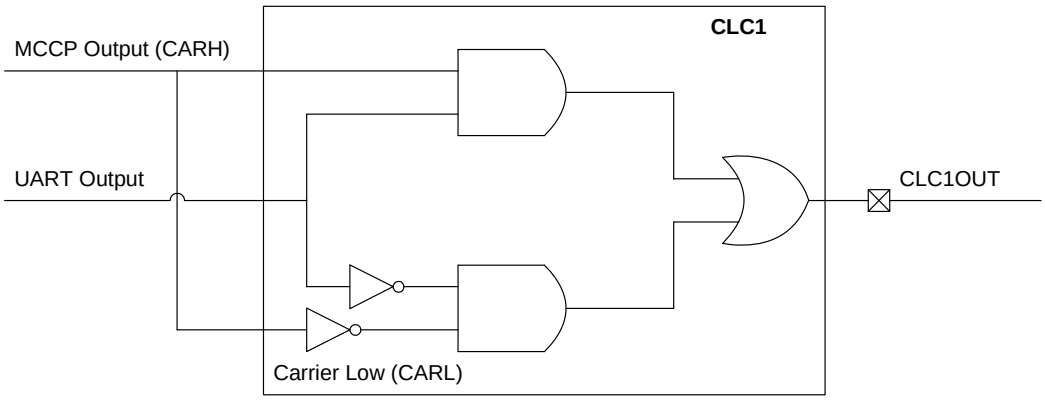


PHASE-SHIFT KEYING (PSK)

In PSK modulation, logic ‘1’ is modulated with the carrier wave of some phase, while logic ‘0’ is modulated with the same carrier wave but of a different phase.

Figure 16 depicts the configuration of CLC1 to generate PSK.

FIGURE 16: PSK MODULATION IN DSM USING CLC



Note: Inverter operation shown in the figure is done using the CLC register bits.

The peripherals required for this application are:

- CLC1
- UART data as the modulator signal
- MCCP output as the carrier signal

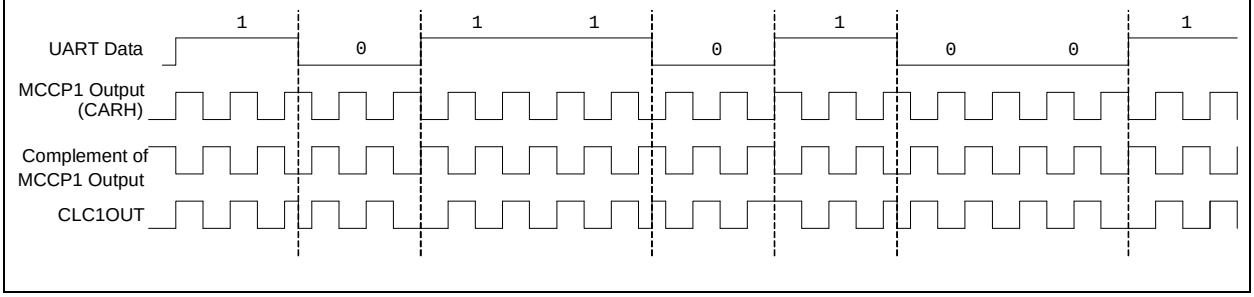
Note:	The UART and MCCP outputs are used as an example for the modulator signal and carrier signal, respectively. However, it is possible to choose other sources of modulator and carrier signals.

Configuring UART: The UART module is configured to transmit the required data.

Configuring MCCP1: The MCCP1 carrier signal is configured to generate an output of the desired frequency. The MCCP1 output is internally fed as an input to the AND gates of CLC1 AND-OR.

Configuring CLC1 to Modulate UART Transmitted Data: CLC1 is configured in AND-OR mode. The MCCP1 output is used as the CARH signal to modulate logic ‘1’ and is ANDed with the UART data. The complement of the MCCP1 output is used as the CARL signal to modulate logic ‘0’ and is ANDed with the complement of the UART data. Both are combined with the OR gate to produce an output on the CLC1OUT pin, which is the required PSK modulated data. CLC1OUT is routed to the physical layer of the subsequent communication interface. Figure 17 shows different signals for PSK.

FIGURE 17: PSK USING CLC1 AND CLC2



APPLICATION 4: MULTIPLE PARAMETER MONITORING

Often, applications require monitoring of different parameters, such as temperature, pressure and humidity, at the same time. If these parameters should start crossing the upper and lower thresholds, it would be necessary to take immediate action. Else, it could be catastrophic as it can damage the entire system.

This application illustrates the use of CLC in monitoring multiple parameters.

The advantages of using CLC for monitoring multiple parameters are:

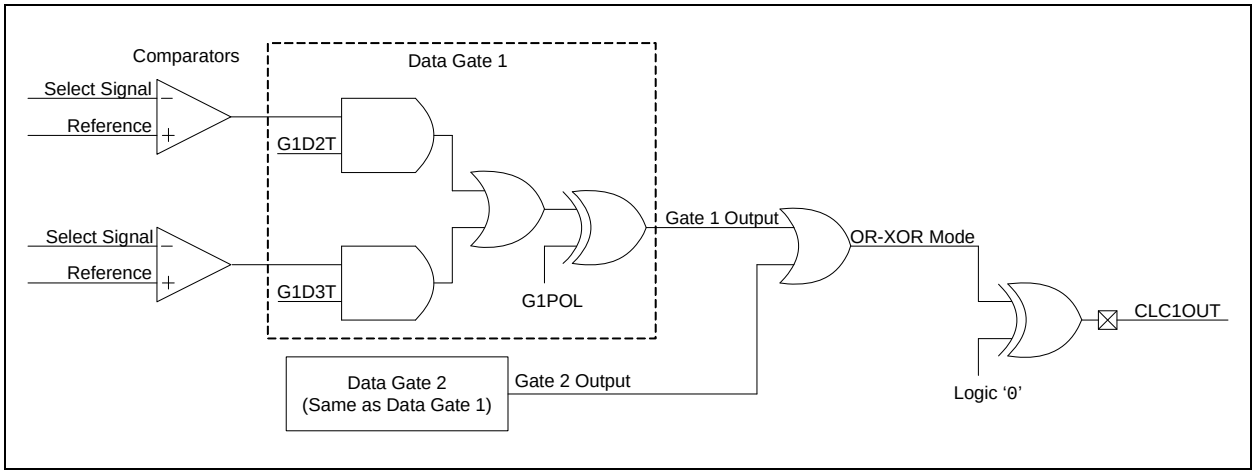
- Multiple comparators are available as source inputs to the CLC. In a microcontroller, a comparator can be utilized to monitor only one parameter; the output of multiple comparators can be combined using the CLC to monitor multiple parameters.
- Necessary action can be taken when any or all of the monitored parameters exceed a certain limit.

Figure 18 shows configuration of the CLC to monitor two different parameters.

The peripherals required for this application are:

- CLC1
- Comparator 1
- Comparator 2

FIGURE 18: MULTIPLE PARAMETER MONITORING USING CLC



Configuring Comparators: Comparators are configured for a predetermined reference voltage with the other input being the parameter to be monitored.

Configuring CLC1: CLC1 is configured in OR-XOR mode. The output of the comparators is internally fed as an input to the data gates of CLC1 (see Figure 18), which is a combination of a group of AND gates and an OR gate. The output of this combination is fed as an input to the OR gate (this OR gate is provided by the CLC1 peripheral's OR-XOR mode). If one of the comparator outputs is high, then the CLC1OUT pin becomes high. The CLC1 interrupt can then be used for further processing of CLC1OUT. In Figure 18, G1D2T and G1D3T are Gate 1 register bits for selecting Data 2 and Data 3. For more information on data bits and Data Gate 1 to Data Gate 4, refer to the specific device data sheet.

If one more parameter is required to be monitored, then another comparator can be used. To get the configuration shown in Figure 18 to work, the Gate 3 and Gate 4 outputs should always be held at the ground level. Hence, one of the inputs to the XOR gate in the OR-XOR mode is always at logic '0'. Therefore, depending on the other input to the XOR gate, the CLC1OUT pin changes.

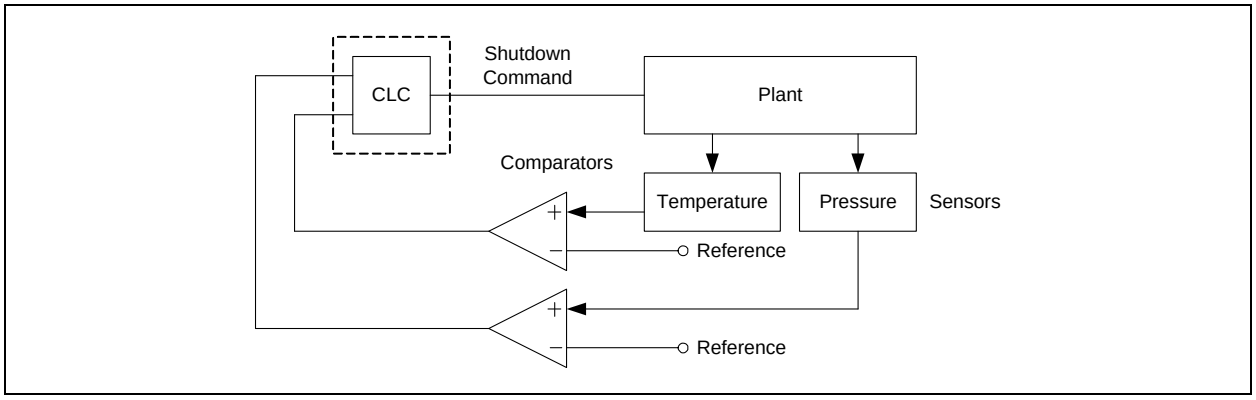
Usage Examples

Two examples for using CLC in multiple parameter monitoring are discussed in the following sections.

USAGE EXAMPLE 1: MONITORING TEMPERATURE AND PRESSURE IN AN INDUSTRIAL PLANT

Figure 19 shows an industrial plant having an analog temperature and pressure sensors for monitoring their values within the plant. The comparators are calibrated for the required reference threshold voltage. If the plant is required to be shut down when either of the parameters exceeds the threshold, then the CLC can be configured as shown in Figure 19.

FIGURE 19: MONITORING TEMPERATURE AND PRESSURE IN AN INDUSTRIAL PLANT USING CLC



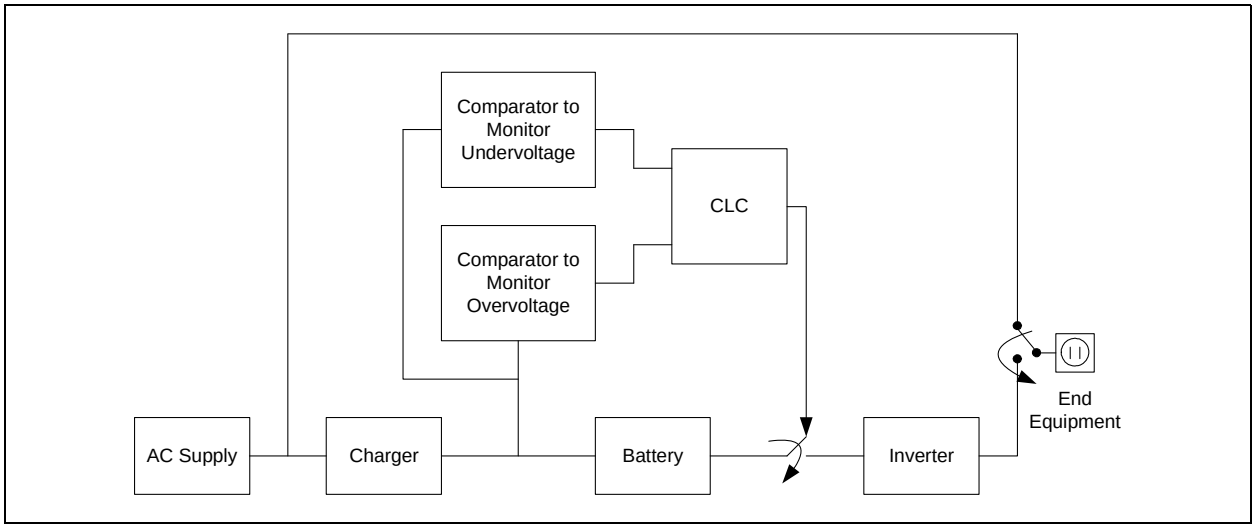
USAGE EXAMPLE 2: MONITORING VOLTAGE LEVELS IN AN OFFLINE UNINTERRUPTIBLE POWER SUPPLY

An Uninterruptible Power Supply (UPS) is a power supply that includes a battery to maintain power in the event of a power outage.

An offline UPS monitors the power line and switches to battery power as soon as it detects a problem.

The protected equipment, such as a Personal Computer, is normally connected directly to the incoming utility power. Figure 20 shows the monitoring of under/overvoltage of an AC supply using the CLC.

FIGURE 20: MONITORING UNDER/OVERVOLTAGE USING CLC



When the incoming voltage falls below, or rises above, a predetermined voltage level, the offline UPS turns on its internal DC-AC inverter circuitry, which is powered from an internal storage battery. The UPS then mechanically switches the connected equipment on to its DC-AC inverter output.

APPLICATION 5: NRZ TO RZ ENCODING

A digital signal is a sequence of discrete voltage pulses. In telecommunication, there are several encoding techniques to map the data bits to its signal element; some of them include:

- NRZ encoding
- RZ encoding
- Manchester encoding

A Non-Return-to-Zero (NRZ) encoding is a form of digital transmission in which the logic '1's are represented by a positive voltage, while logic '0's are represented by a negative voltage or ground. Figure 21 shows a representation of data bits, 1 0 1 1 0, as NRZ encoding.

A Return-to-Zero (RZ) encoding is a form of digital transmission, where the signal transitions (returns) to logic '0' from logic '1', in the middle of each pulse, to represent '1' and remains at zero to represent logic '0'. Figure 22 shows the representation of data bits, 1 0 1 1 0, as RZ encoding.

FIGURE 21: NRZ SIGNAL

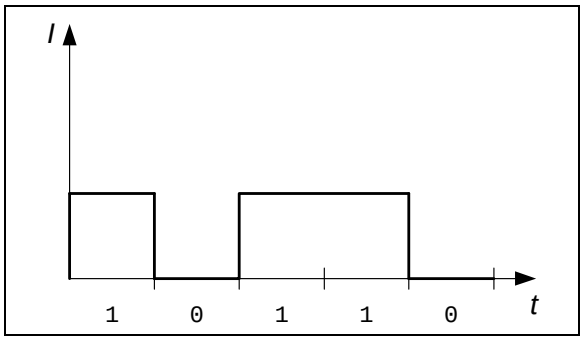


FIGURE 22: RZ SIGNAL

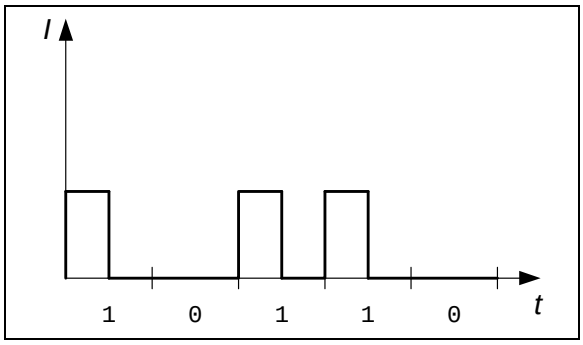
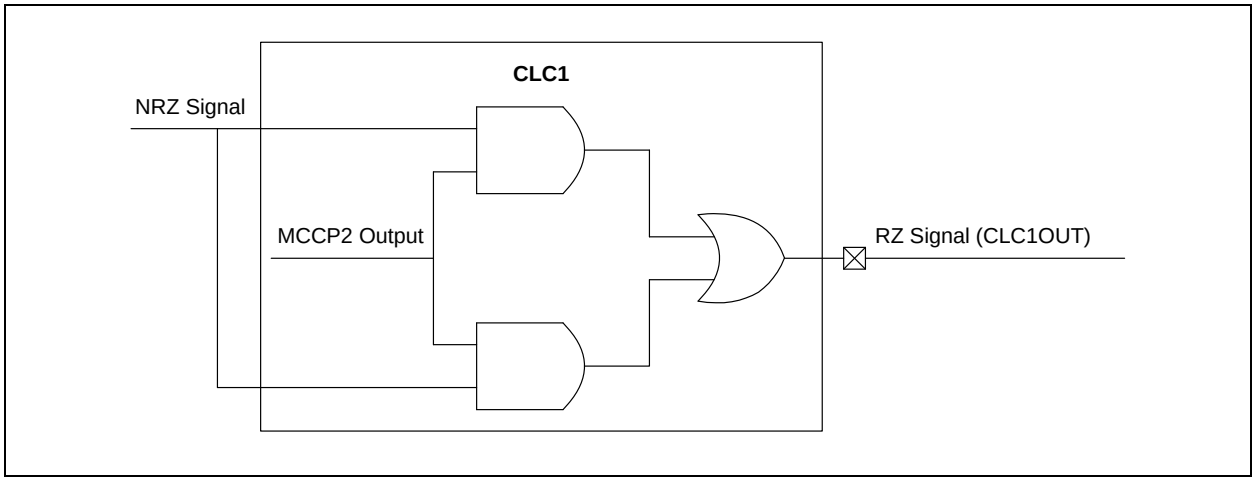


Figure 23 depicts the configuration of CLC to convert NRZ to RZ encoding.

The peripherals required for this application are:

- CLC1
- MCCP2

FIGURE 23: NRZ-RZ CONVERSION USING CLC

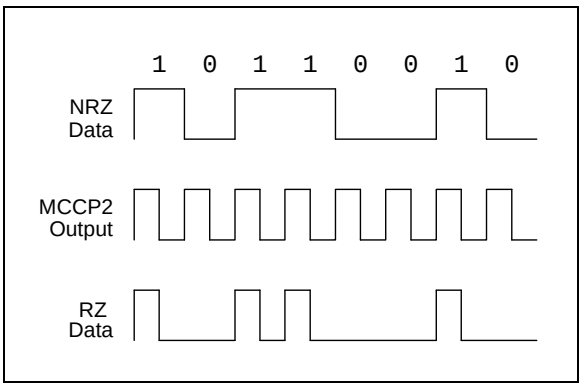


Configuring MCCP2: Assuming ‘T’ as the bit time of the NRZ encoding, MCCP2 is configured to generate a high for half a bit time (that is, T/2) and low for the remaining T/2. The MCCP2 is configured in Trigger mode with CLC1 as the trigger source. This ensures that NRZ is combined with the MCCP2 and generates the RZ encoding.

Note:	An IC can be used to measure the bit time of the NRZ encoding if it is unknown.

CLC1 to Generate RZ Encoding: NRZ encoding is fed as the source input to the CLCINA (or CLCINB) pin. The MCCP2 output is internally fed as the input to CLC1. These two sources are combined by CLC1, which is configured in AND-OR mode. Thus, with MCCP2 as the reference clock, CLC1 generates an RZ encoding. Figure 24 shows the timing diagram for NRZ-RZ conversions.

FIGURE 24: NRZ-RZ CONVERSION TIMING DIAGRAM

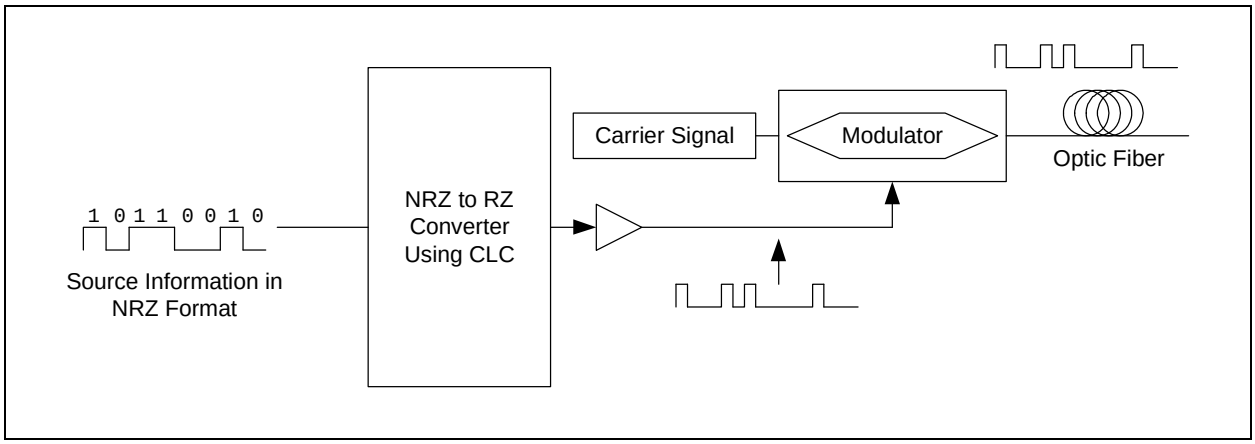


Usage Example: Optical Communication

The NRZ is a standard encoding format for optical communications. However, it is susceptible to impairments in the fiber, which limits the distance traveled by the signal.

An NRZ-RZ converter, using the CLC, can be used to obtain an RZ encoding and transmit it through optic fibers over long distances. Figure 25 shows transmission of RZ encoding through optic fibers.

FIGURE 25: TRANSMISSION OF RZ ENCODING THROUGH OPTIC FIBERS



APPLICATION 6: 2x1 MULTIPLEXER

Multiplexing is a generic term used to describe the operation of sending one or more analog or digital signals over a common transmission line at different times or speeds. In digital electronics, multiplexers (MUX) are also known as data selectors, as they can select one input out of multiple inputs and transmit it as the output. They are used when a single data line is required to carry two or more different digital signals.

A 2x1 MUX is used to select one input from the two available inputs. Thus, it requires a select signal to choose between the two inputs. The general logic diagram of a 2x1 MUX is shown in Figure 26.

The Boolean equation is:

$$Y = I_0 S'_0 + I_1 S_0$$

This application illustrates the process of implementing a 2x1 MUX using the CLC.

FIGURE 26: LOGIC DIAGRAM OF 2x1 MUX

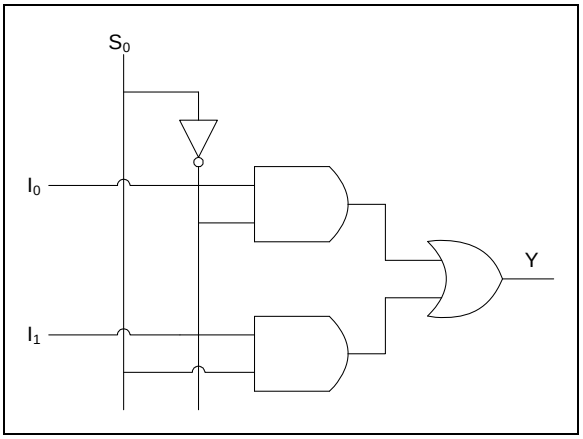
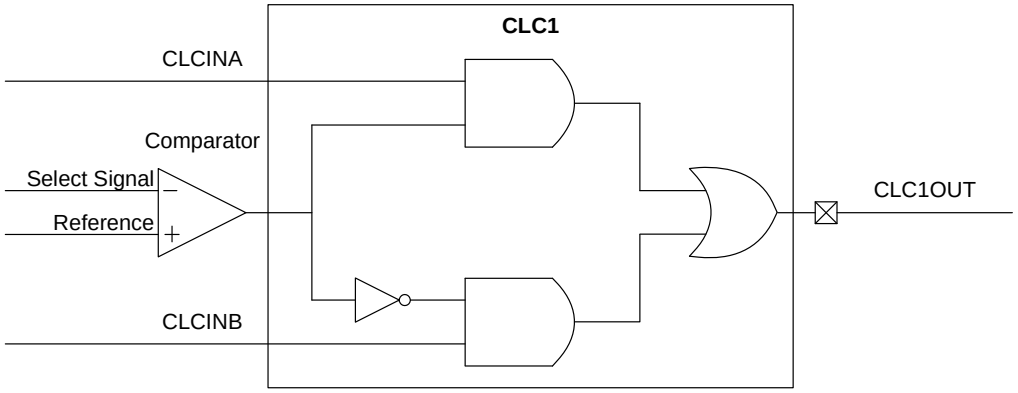


Figure 27 depicts the configuration of CLC to use it as a MUX.

The peripherals required for this application are:

- CLC1
- Comparator

FIGURE 27: MULTIPLEXER USING CLC



Note: Inverter operation shown in the figure is done using the CLC register bits.

Comparator1 as Select Signal: Since there are only two input/output pins for the CLC, the Comparator 1 output can be used as the select signal. Comparator 1 is configured with the DAC output as the reference voltage at the middle of VDD. The output of Comparator 1 is used as the select signal for the MUX. If the source signal input to Comparator 1 is low, then the Comparator 1 output is high. If the source signal input to Comparator 1 is high, then the Comparator 1 output is low.

CLC1 as MUX: CLC1 is configured in AND-OR mode with the Comparator 1 output being internally routed as the select signal. The source signals are fed as an input to CLCINA and CLCINB. If the Comparator 1 output is high, then the signal fed as an input to CLCINA is output on CLC1OUT. Else, if the Comparator 1 output is low, then the signal fed as an input to CLCINB is output on CLC1OUT.

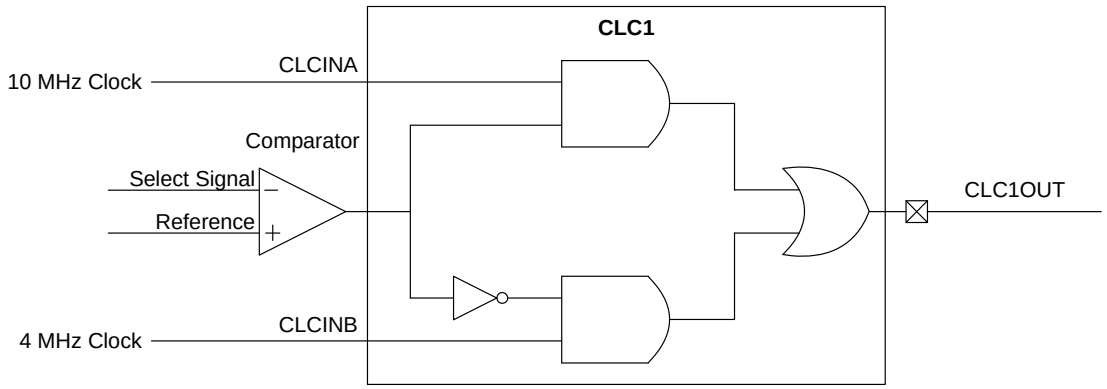
TABLE 1: CLC OUTPUT BASED ON SELECT SIGNAL

Comparator 1 Output (Select Signal)	Output
0	CLCINB (Source 1)
1	CLCINA (Source 2)

Usage Example: Selecting Between Two Different Clock Sources

A two-input MUX could be used in a digital system that uses two different master clock signals: a high-speed clock (e.g., 10 MHz) in one mode and a slow-speed clock (e.g., 4 MHz) for the other. As shown in Figure 28, the 10 MHz clock would be tied to CLCINA and the 4 MHz clock would be tied to CLCINB. A signal from Comparator 1 would select the master clock of the system.

FIGURE 28: SELECTING DIFFERENT CLOCK SOURCES



Note: Inverter operation shown in the figure is done using the CLC register bits.

SUMMARY

The addition of a CLC to the Microchip set of peripherals allows users to design a simple peripheral that can interface with the PIC® microcontroller. This extends the capabilities of PIC MCU devices. Combining outputs of different peripherals and the input pins, using configurable gates enables and the enhancing capabilities of the existing peripherals as well, thus expands the horizon of applications a peripheral can accomplish.

Since the logic functions implemented in the hardware have faster event response compared to the logic functions implemented in the software, the CLC gives the advantage of faster response to users. It provides a higher level of integration without the need of external logic gates to implement the logic functions, hence it can reduce the size of a PCB. It also helps in combining various input source signals using different logic gates to produce altogether different signals.

There is a wide range of applications that can be implemented using CLC; a few are discussed in this document. Microchip encourages users to explore other possibilities of using CLC.

REFERENCES

- *"Configurable Logic Cell Tips 'n Tricks"*, https://ww1.microchip.com/downloads/en/DeviceDoc/41631B.pdf
- **"Configurable Logic Cell (CLC)"** in the *"dsPIC33/PIC24 Family Reference Manual"*, https://ww1.microchip.com/downloads/en/DeviceDoc/33949a.pdf
- AN1779, *"Sensored Single-Phase BLDC Motor Driver Using PIC16F1613"*, https://ww1.microchip.com/downloads/en/AppNotes/00001779A.pdf
- AN1606, *"Using the Configurable Logic Cell (CLC) to Interface a PIC16F1509 and WS2811 LED Driver"*, https://ww1.microchip.com/downloads/en/AppNotes/00001606A.pdf

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