PIC16(L)F18313/18323

PIC16(L)F18313/18323 Family
Silicon Errata and Data Sheet Clarification

The PIC16(L)F18313/18323 family devices that you have received conform functionally to the current Device Data Sheet (DS40001799**A**), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in Table 1. The silicon issues are summarized in Table 2.

The errata described in this document will be addressed in future revisions of the PIC16(L)F18313/18323 silicon.

Note:	This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated in the last column of Table 2 apply to the current silicon revision (**A3**).

Data Sheet clarifications and corrections start on page 5, following the discussion of silicon issues.

The silicon revision level can be identified using the current version of MPLAB® IDE and Microchip's programmers, debuggers, and emulation tools, which are available at the Microchip corporate web site (www.microchip.com).

For example, to identify the silicon revision level using MPLAB IDE in conjunction with a hardware debugger:

1. Using the appropriate interface, connect the device to the hardware debugger.
2. Open an MPLAB IDE project.
3. Configure the MPLAB IDE project for the appropriate device and hardware debugger.
4. Based on the version of MPLAB IDE you are using, do one of the following:
   a) For MPLAB IDE 8, select *Programmer > Reconnect*.
   b) For MPLAB X IDE, select *Window > Dashboard* and click the **Refresh Debug Tool Status** icon ( ).
5. Depending on the development tool used, the part number *and* Device Revision ID value appear in the **Output** window.

Note:	If you are unable to extract the silicon revision level, please contact your local Microchip sales office for assistance.

The DEVREV values for the various PIC16(L)F18313/18323 silicon revisions are shown in Table 1.

TABLE 1: SILICON DEVREV VALUES

Part Number	Device ID(1)	Revision ID for Silicon Revision(2)
		A3
PIC16F18313	3034h	2003h
PIC16LF18313	3036h	2003h
PIC16F18323	3035h	2003h
PIC16LF18323	3037h	2003h

Note 1: The Device IDs (DEVID and DEVREV) are located at addresses 8006h and 8005h, respectively. They are shown in hexadecimal in the format "DEVID DEVREV".

2: Refer to the *"PIC16(L)F183XX Memory Programming Specification"* (DS40001738) for detailed information on Device and Revision IDs for your specific device.

TABLE 2: SILICON ISSUE SUMMARY

Module	Feature	Item Number	Issue Summary	Affected Revisions
				A3
Oscillators	Register Reset Values	1.1	Reset value of OSCTUNE register is 0x20.	X
Oscillators	32 MHz Clock	1.2	32 MHz Internal Clock Signal is not stable.	X
Oscillators	Fail-Safe Clock Monitor (FSCM)	1.3	The FSCM may fail to trigger.	X
Oscillators	Status Flag	1.4	PLLR bit of OSCSTAT1 register is incorrectly cleared.	X
EUSART	Transmit	2.1	TX pin driven low.	X
Master Synchronous Serial Port (MSSP)	SPI Slave Mode	3.1	Slave Select release during Sleep corrupts data.	X
Master Synchronous Serial Port (MSSP)	SPI Slave Mode	3.2	Receive data lost when Slave Select enable occurs just before Sleep execution.	X
Master Synchronous Serial Port (MSSP)	SPI Slave Mode	3.3	WCOL improperly set in Sleep.	X

Note 1: Only those issues indicated in the last column apply to the current silicon revision.

Silicon Errata Issues

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated by the shaded column in the following tables apply to the current silicon revision (**A3**).

1. Module: Oscillators

1.1 Register Reset Values

Upon any Power-on Reset (POR), the value in the OSCTUNE register will be 0x20, which is the lowest frequency adjustment allowed.

Work around

On initial start-up or after any Power-on Reset, write a 0x00 value into the OSCTUNE register, restoring the frequency adjustment back to the factory calibrated setting.

Affected Silicon Revisions

A3							
X							

1.2 32 MHz Clock

When the 32 MHz internal oscillator frequency is selected by writing '110' to either the RSTOSC<2:0> bits of Configuration Word 1 or the NOSC<2:0> bits of OSCCON1 and writing '0111' or '1xxx' to the HFFRQ<3:0> bits of OSCFRQ, the oscillator will fail to lock at 32 MHz and may become unstable.

Work around

1. To achieve a 32 MHz internal oscillator upon power-up or Reset, write '000' to the RSTOSC<2:0> bits of Configuration Word 1, which automatically selects the 32 MHz INTOSC with an internal 2xPLL, sets the HFFRQ<3:0> bits to '0110', and sets the NDIV<3:0> bits of OSCCON1 to '0000' (1:1 divider ratio).

2. To achieve a 32 MHz internal oscillator from an established clock source, write '000' to the NOSC<2:0> bits and '0000' to the NDIV<3:0> bits of OSCCON1, and write '0110' to the HFFRQ<3:0> bits of OSCFRQ.

HFFRQ<3:0>	Nominal Freq. (MHz) (NOSC = 110)	2xPLL Freq. (MHz) (NOSC = 000)
0000	1	Reserved
0001	2	
0010	Reserved	
0011	4	
0100	8	16
0101	12	24
0110	16	32
0111	Reserved	Reserved
1xxx	Reserved	Reserved

Affected Silicon Revisions

A3							
X							

1.3 Fail-Safe Clock Monitor (FSCM)

The Fail-Safe Clock Monitor may fail to trigger with the loss of the external clock signal when the 4x PLL is enabled. This includes all external clock modes, LP, XT, HS, ECL, ECM, and ECH.

Work around

None.

Affected Silicon Revisions

A3							
X							

1.4 Status Flag

When switching from the Internal Oscillator with PLL enabled to an external oscillator with PLL enabled and the clock switch fails, the PLL ready (PLLR) bit of the OSCSTAT1 register is incorrectly cleared.

Work around

None.

Affected Silicon Revisions

A3							
X							

2. Module: EUSART

2.1 Transmit

When the EUSART module is enabled (SPEN = 1) with the transmit function disabled (TXEN = 0), the TX assigned pin is driven low.

Work around

Load the desired logic level into the corresponding LATx register and assign the I/O function via the PPS output register.

Affected Silicon Revisions

A3							
X							

3. Module: Master Synchronous Serial Port (MSSP)

3.1 SPI Slave Data Corruption During Sleep

When the MSSP module is configured in SPI Slave mode with $\overline{SS}$ pin control enabled (SSPM = 0100) and the device is in Sleep mode during SPI activity, if the SPI master releases the $\overline{SS}$ line ($\overline{SS}$ goes high) before the device wakes from Sleep and updates SSPBUF, the received data will be lost.

Work around

Method 1: The SPI master must wait a minimum of parameter SP83 (1.5 TCY + 40 nS) after the last SCK edge AND the additional wake-up time from Sleep (device dependent) before releasing the $\overline{SS}$ line.

Method 2: If both the master and slave devices have an available pin, once the slave has completed the transaction and BF or SSPIF is set, the slave could toggle an output to inform the master that the transaction is complete and that it is safe to release the $\overline{SS}$ line.

Affected Silicon Revisions

A3							
X							

3.2 SPI Slave Data Corruption During Sleep

When the MSSP module is configured in SPI Slave mode with $\overline{SS}$ pin control enabled (SSPM = 0100) and the device is in Sleep mode during SPI activity, if the SPI master enables $\overline{SS}$ ($\overline{SS}$ goes low) within 1 TCY before Sleep is executed, the data written into the SSPBUF by the slave for transmission will remain in the SSPBUF, and the byte received by the slave will be completely discarded. The MSb of the data byte that is currently loaded into SSPBUF will be transmitted on each of the eight SCK clocks, resulting in either a 0x00 or 0xFF to be incorrectly transmitted. This issue typically occurs when the device wakes up from Sleep to process data and immediately goes back to Sleep during the next transmission.

Work around

The SPI Slave must wait a minimum of 2.25*TCY from the time the $\overline{SS}$ line becomes active ($\overline{SS}$ goes low) before executing the Sleep command.

Affected Silicon Revisions

A3							
X							

3.3 WCOL Bit Improperly Set During Sleep

When the MSSP module is configured with either of the Slave modes listed below and Sleep is executed during transmission, the WCOL bit is erroneously set. Although the WCOL bit is set, it does not cause a break in transmission or reception.

Mode 1: SPI Slave mode with $\overline{SS}$ disabled (SSPM = 0101) and CKE = 0.

Mode 2: SPI Slave mode with $\overline{SS}$ enabled (SSPM = 0100) and $\overline{SS}$ is not set and then cleared before each consecutive transmission. This typically occurs during multiple byte transmissions in which the master does not release the $\overline{SS}$ line until all transmission has completed.

Work around

Method 1: The WCOL bit can be ignored since the issue does not interfere with MSSP hardware.

Method 2: Clear the SSPEN after each transaction, then set SSPEN before the next transaction.

Affected Silicon Revisions

A3							
X							

Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS40001799**A**):

Note:	Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

1. Module: CCP

In **Section 28.2**, a note box will be added as follows:

Note:	When the CCP is configured in Compare mode using the 'toggle output on match' setting (CCPxMODE<3:0> bits = 0010) and the reference timer is set for an input clock prescale other than 1:1, the output of the CCP will toggle multiple times until finally settling a '0' logic level. To avoid this, the timer input clock prescale select bits must be set to a 1:1 ratio (TxCKPS = 00).

2. Module: Oscillators

In **Section 6.5**, the HFINTOSC Frequency Selection Register (OSCFRQ) will be modified as follows:

REGISTER 6-6: OSCFRQ: HFINTOSC FREQUENCY SELECTION REGISTER

U-0	U-0	U-0	U-0	**R/W-0/0**	R/W-**1/1**	R/W-**1/1**	R/W-**0/0**
—	—	—	—	**HFFRQ<3:0>**			
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-**4** Unimplemented: Read as '0'.

bit **3**-0 **HFFRQ<3:0>:** HFINTOSC Frequency Selection bits

HFFRQ<3:0>	Nominal Freq. (MHz) (NOSC = 110)	2xPLL Freq. (MHz) (NOSC = 000)
0000	1	**Reserved**
0001	2	
0010	Reserved	
0011	4	
0100	8	16
0101	12	24
0110	16	32
0111	**32**	Reserved
1xxx	**32**	**Reserved**

3. Module: Resets

In **Section 5.12**, Bit 6 of the Brown-out Reset Control Register (BORCON) will be modified as follows:

REGISTER 5-1: BORCON: BROWN-OUT RESET CONTROL REGISTER

R/W-1/u	R/W-0/0	U-0	U-0	U-0	U-0	U-0	R-q/u
SBOREN(1)	Reserved	—	—	—	—	—	BORRDY
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	q = Value depends on condition

bit 7 SBOREN: Software Brown-out Reset Enable bit(1)
If BOREN <1:0> in Configuration Words ≠ 01:
SBOREN is read/write, but has no effect on the BOR.
If BOREN <1:0> in Configuration Words = 01:
1 = BOR Enabled
0 = BOR Disabled

bit 6 **Reserved. Bit must be maintained as '0'.**

bit 5-1 Unimplemented: Read as '0''.

bit 0 BORRDY: Brown-out Reset Circuit Ready Status bit
1 = The Brown-out Reset circuit is active
0 = The Brown-out Reset circuit is inactive

Note 1: BOREN<1:0> bits are located in Configuration Words.

4. Module: Power-Saving Operation

In **Section 8.3**, Bit 0 of the Voltage Regulator Control Register (VREGCON) will be modified as follows:

REGISTER 8-1: VREGCON: VOLTAGE REGULATOR CONTROL REGISTER(1)

U-0	U-0	U-0	U-0	U-0	U-0	R/W-0/0	R/W-1/1
—	—	—	—	—	—	VREGPM	**Reserved**
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7-2 Unimplemented: Read as ‘0’

bit 1 **VREGPM:** Voltage Regulator Power Mode Selection bit
- 1 = Low-Power Sleep mode enabled in Sleep(2)
  Draws lowest current in Sleep, slower wake-up
- 0 = Normal-Power mode enabled in Sleep(2)
  Draws higher current in Sleep, faster wake-up

bit 0 Reserved: Read as ‘1’. Maintain this bit set.

Note 1: **PIC16(L)F18313/18323** only.
2: See **Section 34.0 “Electrical Specifications”**.

5. Module: Electrical Specifications

In **Section 34**, Table 34-11: Reset, Watchdog Timer, Oscillator Start-up Timer, Power-up Timer, Brown-out Reset and Low-Power Brown-out Reset Specification, will be modified as follows:

TABLE 34-11: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER, POWER-UP TIMER, BROWN-OUT RESET AND LOW POWER BROWN-OUT RESET SPECIFICATIONS

Standard Operating Conditions (unless otherwise stated)							
Param. No.	**Sym.**	**Characteristic**	**Min.**	**Typ.†**	**Max.**	**Units**	**Conditions**
RST01	TMCLR	$\overline{MCLR}$ Pulse Width Low to ensure Reset	2	—	—	µs	
RST02	TIOZ	I/O high-impedance from Reset detection	—	—	2	µs	
RST03	TWDT	Watchdog Timer Time-out Period	10	16	27	ms	16 ms Nominal Reset Time
RST04*	TPWRT	Power-up Timer Period	40	65	140	ms	
RST05	TOST	Oscillator Start-up Timer Period(1,2)	—	1024	—	TOSC	(Note3)
RST06	VBOR	Brown-out Reset Voltage(4)	2.55 2.30 1.80	2.70 2.45 1.90	2.85 2.60 2.10	V V V	BORV = 0 BORV = 1 (PIC16F18325/18345) BORV = 1 (PIC16LF18325/18345)
RST07	VBORHYS	Brown-out Reset Hysteresis	0	25	75	mV	
RST08	TBORDC	Brown-out Reset Response Time	1	3	35	µs	
RST09	VLPBOR	Low-Power Brown-out Reset Voltage	**1.8**	**2.1**	**2.5**	**V**	PIC16(L)F18313/18323

* These parameters are characterized but not tested.

† Data in "Typ." column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Instruction cycle period (TCY) equals four times the input oscillator time base period. All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at "min" values with an external clock applied to the OSC1 pin. When an external clock input is used, the "max" cycle time limit is "DC" (no clock) for all devices.

2: By design.

3: Period of the slower clock.

4: To ensure these voltage tolerances, VDD and VSS must be capacitively decoupled as close to the device as possible. 0.1 µF and 0.01 µF values in parallel are recommended.

6. Module: Oscillators

In Section 6.6, Register 6-1 Note 4 will be modified as follows:

4: When RSTOSC = 110 (HFINTOSC 1 MHz), the NDIV bits will default to '**0100**' upon Reset; for all other NOSC settings the NDIV bits will default to '0000' upon Reset.

APPENDIX A: DOCUMENT REVISION HISTORY

Rev A Document (10/2015)

Initial release of this document.

NOTES:

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
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