SMPS AC/DC Reference Design
User's Guide

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break Microchip's code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.

Trademarks

QUALITY MANAGEMENT SYSTEM
CERTIFIED BY DNV
ISO/TS 16949:2002

Microchip received ISO/TS-16949:2002 certification for its worldwide headquarters, design and wafer fabrication facilities in Chandler and Tempe, Arizona; Gresham, Oregon and design centers in California and India. The Company's quality system processes and procedures are for its PIC® MCUs and dsPIC® DSCs, KEELOQ® code hopping devices, Serial EEPROMs, microperipherals, nonvolatile memory and analog products. In addition, Microchip's quality system for the design and manufacture of development systems is ISO 9001:2000 certified.

SMPS AC/DC REFERENCE DESIGN USER'S GUIDE

Table of Contents

Preface

NOTICE TO CUSTOMERS

All documentation becomes dated, and this manual is no exception. Microchip tools and documentation are constantly evolving to meet customer needs, so some actual dialogs and/or tool descriptions may differ from those in this document. Please refer to our web site (www.microchip.com) to obtain the latest documentation available.

Documents are identified with a "DS" number. This number is located on the bottom of each page, in front of the page number. The numbering convention for the DS number is "DSXXXXXA", where "XXXXX" is the document number and "A" is the revision level of the document.

For the most up-to-date information on development tools, see the MPLAB® IDE on-line help. Select the Help menu, and then Topics to open a list of available on-line help files.

INTRODUCTION

This chapter contains general information that will be useful to know before using the SMPS AC/DC Reference Design. Items discussed in this chapter include:

- Document Layout
- Conventions Used in this Guide
- Warranty Registration
- Recommended Reading
- The Microchip Web Site
- Development Systems Customer Change Notification Service
- Customer Support
- Document Revision History

DOCUMENT LAYOUT

This document describes how to use the SMPS AC/DC Reference Design as a development tool to emulate and debug firmware on a target board. The manual layout is as follows:

- **Chapter 1. "Introduction"** – This chapter introduces the SMPS AC/DC Reference Design and provides an overview of its features and background information.
- **Chapter 2. "Hardware Design"** – This chapter provides a functional overview of the SMPS AC/DC Reference Design and identifies the major hardware components.
- **Chapter 3. "Software Design"** – This chapter provides a functional overview of the software used in the hardware design and identifies the major software components.
- **Chapter 4. "System Operation"** – This chapter provides information on the system operation and setup for the SMPS AC/DC Reference Design.

- **Appendix A. "Board Layouts and Schematics"** – This appendix provides detailed technical drawings and schematic diagrams of the SMPS AC/DC Reference Design.
- **Appendix B. "Test Results"** – This appendix provides information on obtaining the source code referenced in this document.
- **Appendix C. "References"** – This appendix provides detailed information on all external references used throughout this document.

CONVENTIONS USED IN THIS GUIDE

This manual uses the following documentation conventions:

DOCUMENTATION CONVENTIONS

Description	Represents	Examples
Arial font:		
Italic characters	Referenced books	*MPLAB® IDE User's Guide*
	Emphasized text	...is the *only* compiler...
Initial caps	A window	the Output window
	A dialog	the Settings dialog
	A menu selection	select Enable Programmer
Quotes	A field name in a window or dialog	"Save project before build"
Underlined, italic text with right angle bracket	A menu path	*File>Save*
Bold characters	A dialog button	Click **OK**
	A tab	Click the **Power** tab
N'Rnnnn	A number in verilog format, where N is the total number of digits, R is the radix and n is a digit.	4'b0010, 2'hF1
Text in angle brackets < >	A key on the keyboard	Press <Enter>, <F1>
Courier New font:		
Plain Courier New	Sample source code	`#define START`
	Filenames	`autoexec.bat`
	File paths	`c:\mcc18\h`
	Keywords	`_asm, _endasm, static`
	Command-line options	`-Opa+, -Opa-`
	Bit values	`0, 1`
	Constants	`0xFF, 'A'`
Italic Courier New	A variable argument	*`file`*`.o`, where *`file`* can be any valid filename
Square brackets [ ]	Optional arguments	`mcc18 [options]` *`file`* `[options]`
Curly brackets and pipe character: { | }	Choice of mutually exclusive arguments; an OR selection	`errorlevel {0|1}`
Ellipses...	Replaces repeated text	`var_name [, var_name...]`
	Represents code supplied by user	`void main (void) { ... }`

WARRANTY REGISTRATION

Please complete the enclosed Warranty Registration Card and mail it promptly. Sending in the Warranty Registration Card entitles users to receive new product updates. Interim software releases are available at the Microchip web site.

RECOMMENDED READING

This user's guide describes how to use SMPS AC/DC Reference Design. Other useful documents are listed below. The following Microchip documents are available and recommended as supplemental reference resources.

Readme Files

For the latest information on using other tools, read the tool-specific Readme files in the `Readmes` subdirectory of the MPLAB® IDE installation directory. The Readme files contain update information and known issues that may not be included in this user's guide.

Application Notes

The following related SMPS application notes are available for download from the Microchip website:

- AN1106 *"Power Factor Correction in Power Conversion Applications Using the dsPIC® DSC"* (DS01106)
- AN1114 *"Switch Mode Power Supply (SMPS) Topologies (Part I)"* (DS01114)
- AN1207 *"Switch Mode Power Supply (SMPS) Topologies (Part II)"* (DS01207)

THE MICROCHIP WEB SITE

Microchip provides online support via our web site at www.microchip.com. This web site is used as a means to make files and information easily available to customers. Accessible by using your favorite Internet browser, the web site contains the following information:

- **Product Support** – Data sheets and errata, application notes and sample programs, design resources, user's guides and hardware support documents, latest software releases and archived software
- **General Technical Support** – Frequently Asked Questions (FAQs), technical support requests, online discussion groups, Microchip consultant program member listing
- **Business of Microchip** – Product selector and ordering guides, latest Microchip press releases, listing of seminars and events, listings of Microchip sales offices, distributors and factory representatives

DEVELOPMENT SYSTEMS CUSTOMER CHANGE NOTIFICATION SERVICE

Microchip's customer notification service helps keep customers current on Microchip products. Subscribers will receive e-mail notification whenever there are changes, updates, revisions or errata related to a specified product family or development tool of interest.

To register, access the Microchip web site at www.microchip.com, click on Customer Change Notification and follow the registration instructions.

The Development Systems product group categories are:

- **Compilers** – The latest information on Microchip C compilers and other language tools. These include the MPLAB C18 and MPLAB C30 C compilers; MPASM™ and MPLAB ASM30 assemblers; MPLINK™ and MPLAB LINK30 object linkers; and MPLIB™ and MPLAB LIB30 object librarians.
- **Emulators** – The latest information on Microchip in-circuit emulators.This includes the MPLAB ICE 2000 and MPLAB ICE 4000.
- **In-Circuit Debuggers** – The latest information on the Microchip in-circuit debugger, MPLAB ICD 2.
- **MPLAB® IDE** – The latest information on Microchip MPLAB IDE, the Windows® Integrated Development Environment for development systems tools. This list is focused on the MPLAB IDE, MPLAB SIM simulator, MPLAB IDE Project Manager and general editing and debugging features.
- **Programmers** – The latest information on Microchip programmers. These include the MPLAB PM3 and PRO MATE II device programmers and the PICSTART® Plus and PICkit™ 1 development programmers.

CUSTOMER SUPPORT

Users of Microchip products can receive assistance through several channels:

- Distributor or Representative
- Local Sales Office
- Field Application Engineer (FAE)
- Technical Support

Customers should contact their distributor, representative or field application engineer (FAE) for support. Local sales offices are also available to help customers. A listing of sales offices and locations is included in the back of this document.

Technical support is available through the web site at: http://support.microchip.com

DOCUMENT REVISION HISTORY

Revision A (February 2008)

Initial release of this document.

Revision B (November 2008)

This revision of the document includes the following updates:

- Extensive updates have been made throughout the document to reflect the redesign of the software and the hardware to accommodate the 3.3V SMPS dsPIC® DSC device (dsPIC33FJ16GS504)
- Modified contents of **Appendix B. "Test Results"** (previously named **"Source Code"**)
- Updated all board layout diagrams and schematics in **Appendix A. "Board Layouts and Schematics"**

NOTES:

Chapter 1. Introduction

This chapter provides an introduction to the SMPS AC/DC Reference Design and includes the following major topics:

- System Specifications
- Block Diagram
- Multi-Phase Synchronous Buck Converter
- Listing of I/O Signals for Each Block, Type of Signal and Expected Signal Levels

1.1 SYSTEM SPECIFICATIONS

This reference design describes the design of an off-line Switch Mode Power Supply (SMPS) design using an SMPS dsPIC® DSC (dsPIC33FJ16GS504).

The SMPS AC/DC Reference Design works with universal input voltage range and produces three output voltages (12V, 3.3V and 5V). The continuous output rating of the reference design is 300 Watts. This reference design is based on a modular structure having three major block sets as shown in Figure 1-1. Figure 1-2 shows a more detailed block diagram with all functional blocks as implemented on the SMPS AC/DC Reference Design.

The Power Factor Circuit (PFC) converts the universal AC input voltage to constant high-voltage DC, and maintains the sinusoidal input current at high power factor. The Phase-Shift Zero Voltage Transition circuit converts high-voltage DC to intermediate low-voltage DC with isolation from the input AC mains, at high efficiency. The Multi-Phase Synchronous and Single-Phase Synchronous Buck circuit converts intermediate low-voltage DC to very low-voltage DC at high current at high efficiency. The input and output specifications are as follows:

- Input:
  - Input voltage: 85 VAC-265 VAC
  - Input frequency: 45 Hz-65 Hz
- Outputs (individually loaded):
  - Output voltage 1 (*Vo1*) = 12V
  - Output load 1 (*Io1*) = 0A-30A
  - Output voltage 2 (*Vo2*) = 3.3V
  - Output load 2 (*Io2*) = 0A-69A
  - Output voltage 3 (*Vo3*) = 5V
  - Output load 3 (*Io3*) = 0A-23A
- Outputs (simultaneously loaded):
  - Output voltage 2 (*Vo2*) = 3.3V
  - Output load 2 (*Io2*) = 0A-56A
  - Output voltage 3 (*Vo3*) = 5V
  - Output load 3 (*Io3*) = 0A-23A

1.2 BLOCK DIAGRAM

A conventional SMPS must implement PFC if it draws more than 75 watts from the AC Mains. The PFC circuitry draws input current in phase with the input voltage, and the Total Harmonic Distortion (THD) of the input current should be less than 5% at full load. The PFC provides a fixed DC high-output voltage, which needs to be converted to a lower Direct Current (DC) output voltage and isolated with an input mains supply. Figure 1-2 shows a high-level block diagram of the SMPS AC/DC Reference Design. Figure 1-2 shows a detailed block diagram.

The SMPS AC/DC Reference Design operates on universal input voltage and produces multiple DC output voltages. The front-end PFC Boost circuit converts universal AC input voltage to 420 VDC bus voltage. The Phase-Shift Zero Voltage Transition (ZVT) circuit produces 12 VDC output voltage from a 420 VDC bus. The Phase-Shift ZVT converter also provides output voltage isolation from the input AC mains. The Multi-Phase Synchronous Buck converter produces 3.3 VDC @ 69 Amps from the 12 VDC bus. The Single-Phase Buck converter produces 5 VDC @ 23 Amps from the 12 VDC bus.

The following sections in this chapter provide an overview and background of the main power conversion blocks implemented in the SMPS AC/DC Reference Design.

FIGURE 1-1: HIGH-LEVEL SMPS AC/DC REFERENCE DESIGN BLOCK DIAGRAM

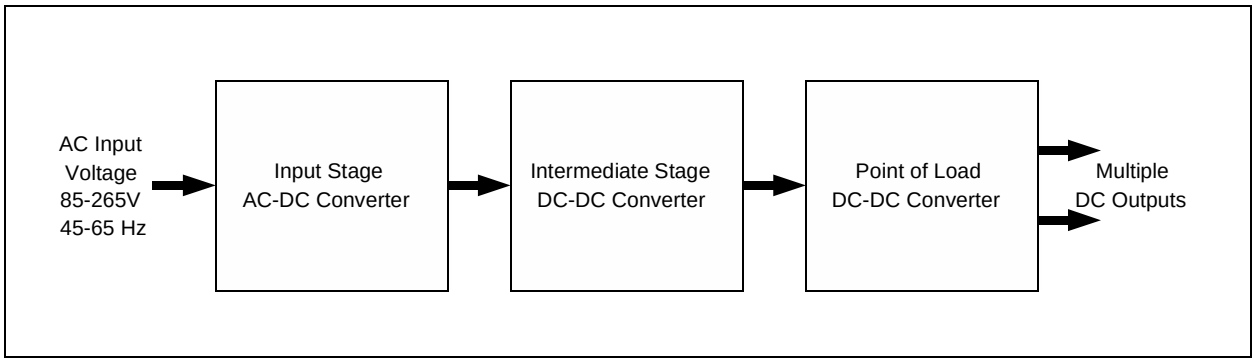
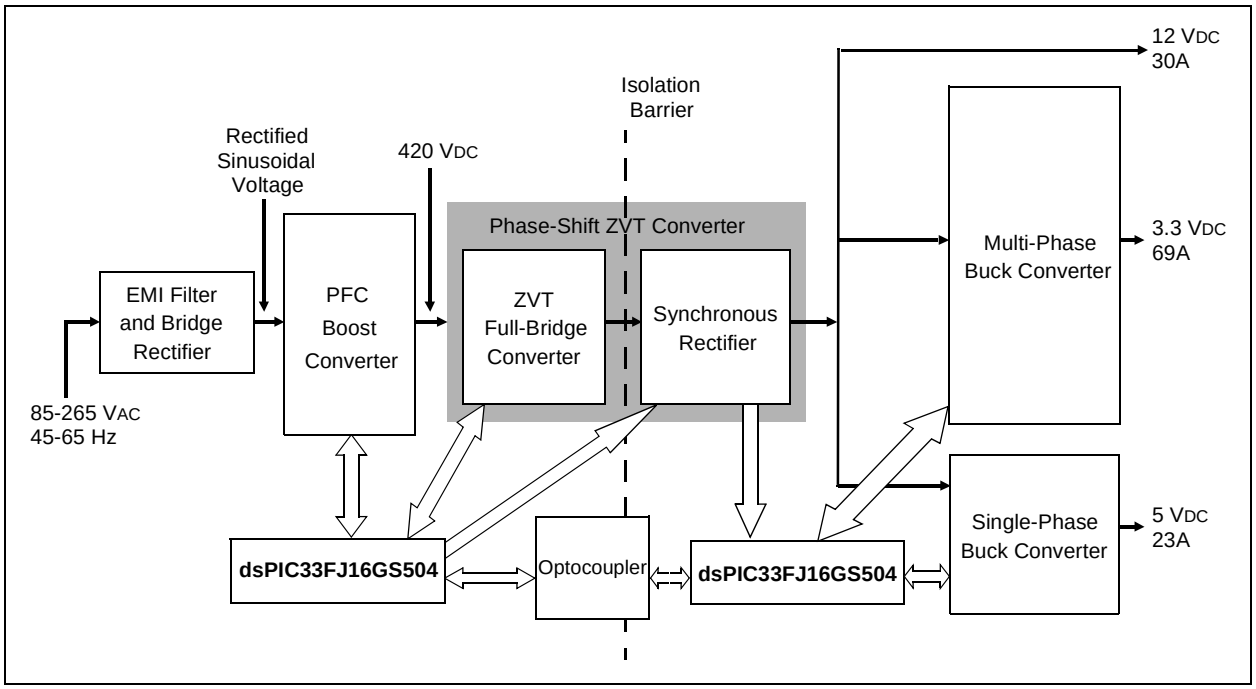


FIGURE 1-2: DETAILED SMPS AC/DC REFERENCE DESIGN BLOCK DIAGRAM



1.2.1 Power Factor Correction (PFC)

Most power conversion applications consist of an AC-to-DC conversion stage immediately following the AC source. The DC output obtained after rectification is subsequently used for further stages. Current pulses with high peak amplitude are drawn from a rectified voltage source with sine wave input and capacitive filtering. Regardless of the load connected to the system, the current drawn is discontinuous and of short duration. Because many applications demand a DC voltage source, a rectifier with a capacitive filter is necessary. However, this results in discontinuous, short duration current spikes.

1.2.1.1 OVERVIEW AND BACKGROUND INFORMATION

Two factors that provide a quantitative measure of the power quality in an electrical system are Power Factor (PF) and Total Harmonic Distortion (THD). The amount of useful power being consumed by an electrical system is predominantly decided by the PF of the system.

To understand PF, it is important to know that power has two components:

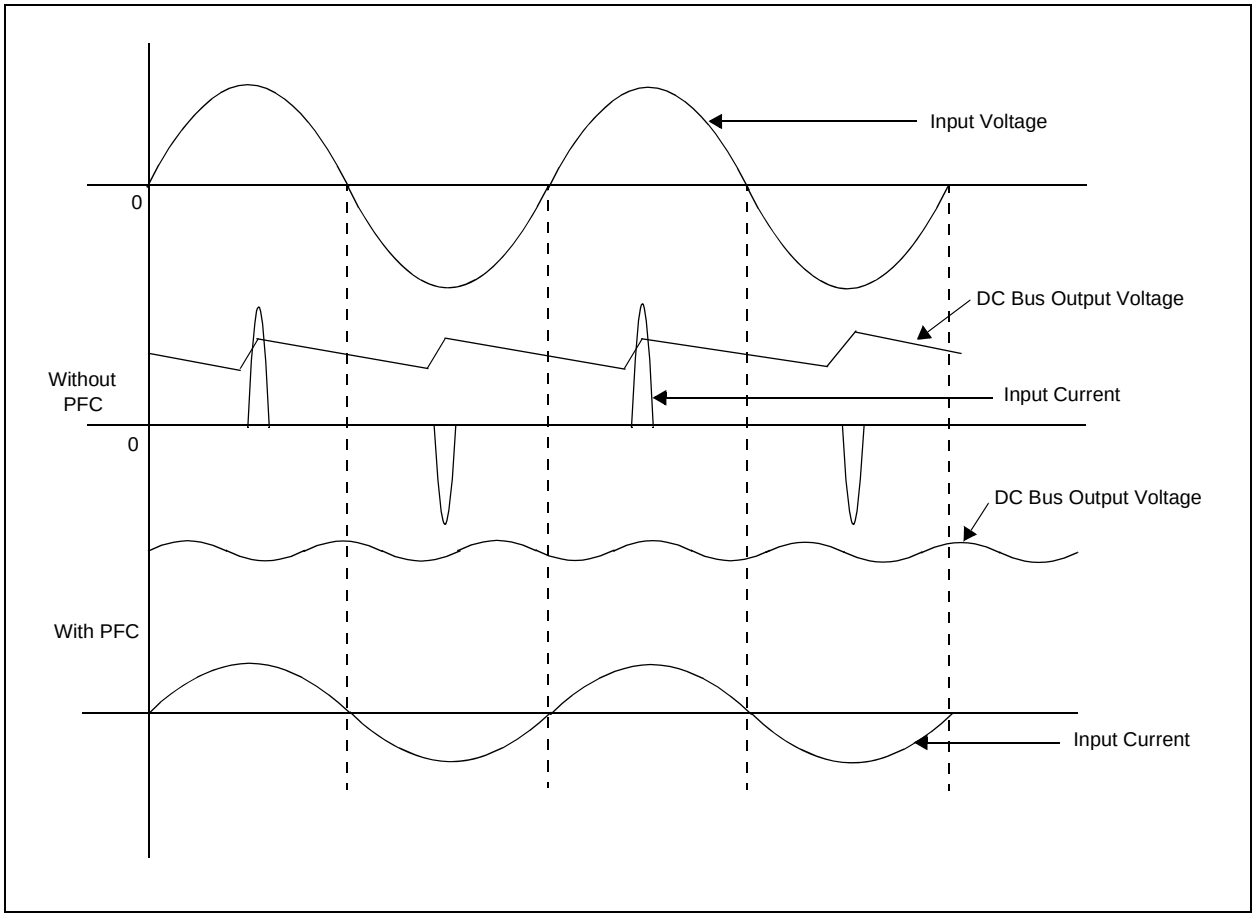
- Working (or Active Power)

  Working Power is the power that is actually consumed and registered on the electric meter at the consumer's location. Working power is expressed in kilowatts (kW), which register as kilowatt hour (kWh) on an electric meter.
- Reactive Power

  Reactive Power is required to maintain and sustain the electromagnetic field associated with the industrial inductive loads such as induction motors driving pumps or fans, welding machines and many more. Reactive Power is measured in kilovolt ampere reactive (kVAR) units. The total required power capacity, including Working Power and Reactive Power, is known as Apparent Power, expressed in kilovolt ampere (kVA) units.

Power Factor is a parameter that gives the amount of working power used by any system in terms of the total apparent power. Power Factor becomes an important measurable quantity because it often results in significant economic savings. Typical waveforms of current with and without PFC are shown in Figure 1-3.

FIGURE 1-3: INPUT CURRENT WAVEFORM WITH AND WITHOUT PFC



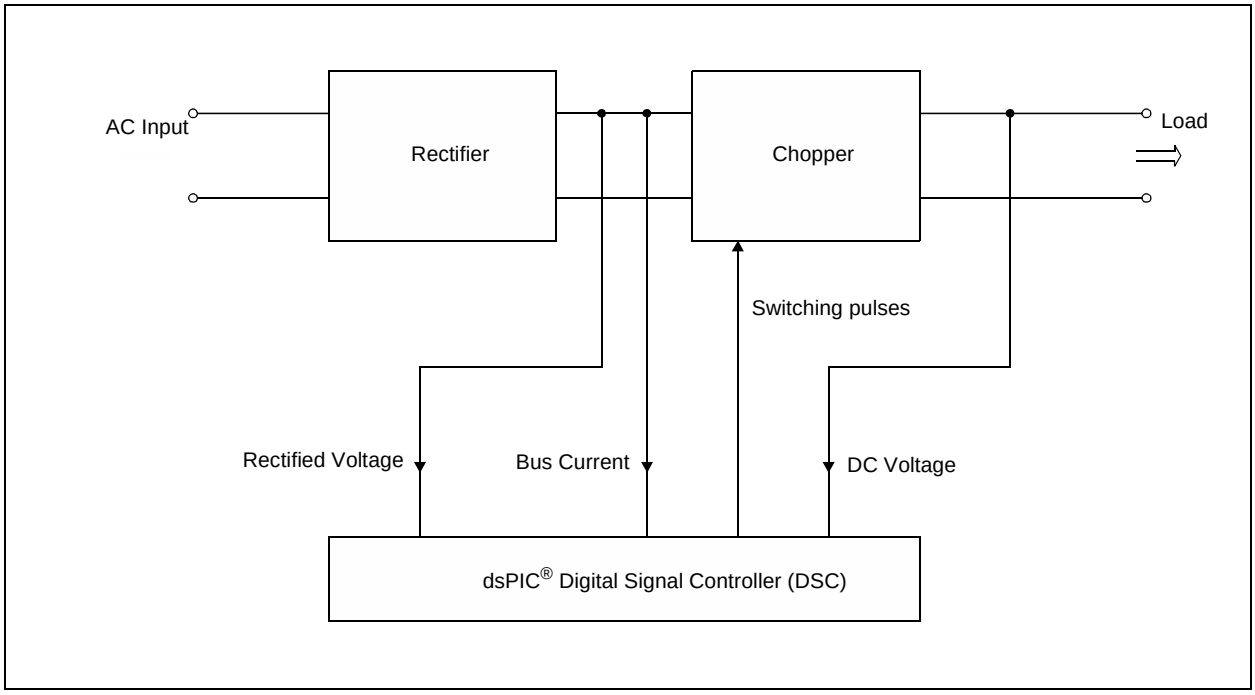
These waveforms illustrate that PFC can improve the input current drawn from the mains supply and reduce the DC bus voltage ripple. The objective of PFC is to make the input to a power supply look like a simple resistor. The PFC circuitry provides a power factor that is nearly equal to unity with very low current THD (< 5%).

Figure 1-4 shows a block diagram of the AC-to-DC converter stage, which converts the AC input voltage to a DC voltage and maintains sinusoidal input current at a high input Power Factor.

The input rectifier converts the alternating voltage at power frequency into unidirectional voltage. This rectified voltage is fed to the chopper circuit to produce a smooth and constant DC output voltage to the load. The chopper circuit is controlled by the PWM switching pulses generated by the dsPIC DSC device, based on three measured feedback signals:

- Rectified input voltage
- DC bus current
- DC bus voltage

FIGURE 1-4: BLOCK DIAGRAM OF THE COMPONENTS FOR POWER FACTOR CORRECTION



1.2.1.2 PFC TOPOLOGIES

The Power Factor can be achieved with various basic topologies such as Buck, Boost and Buck/Boost.

1.2.1.2.1 Buck PFC Circuit

In a Buck PFC circuit, the output DC voltage is less than the input rectified voltage. Large filters are needed to suppress switching ripples and this circuit produces considerable Power Factor improvement. The switch (MOSFET) is rated to V_{IN} in this case. Figure 1-5 shows the circuit for the Buck PFC stage. Figure 1-6 shows the Buck PFC input current shape.

FIGURE 1-5: BUCK PFC

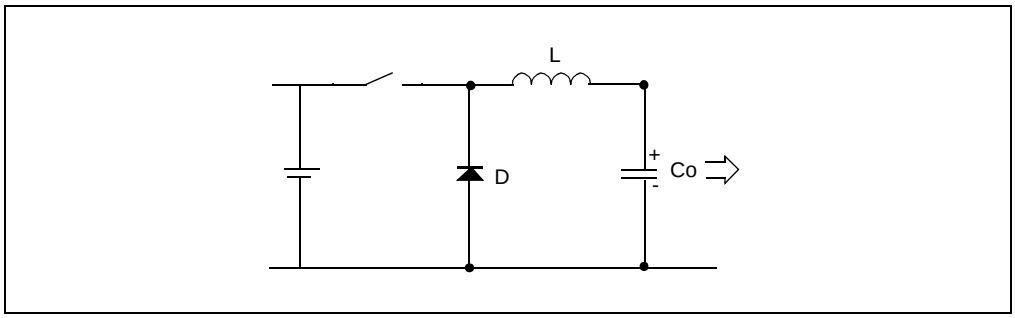
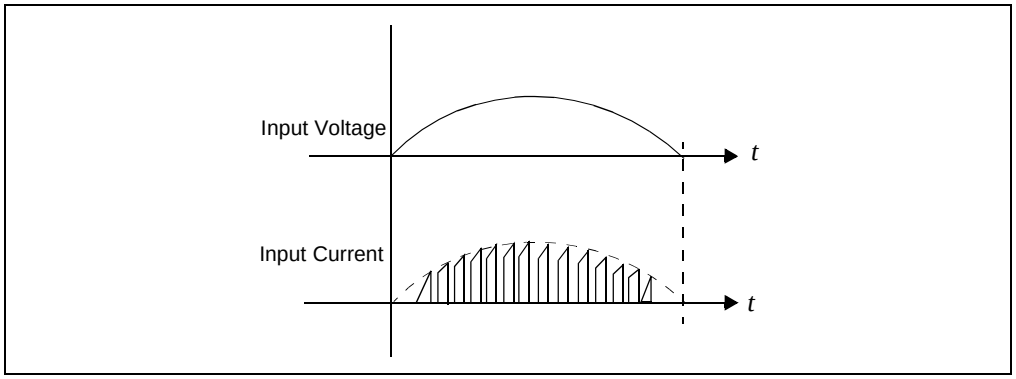


FIGURE 1-6: BUCK PFC INPUT CURRENT SHAPE



1.2.1.2.2 Boost PFC Circuit

The Boost converter produces a voltage higher than the input rectified voltage; therefore, the switch (MOSFET) rating should be rated higher than VOUT. Figure 1-7 shows the circuit for the Boost PFC stage. Figure 1-8 shows the Boost PFC input current shape.

FIGURE 1-7: BOOST PFC

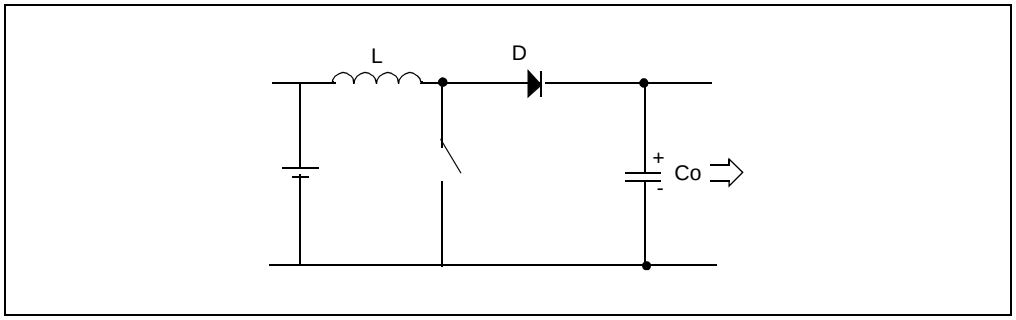
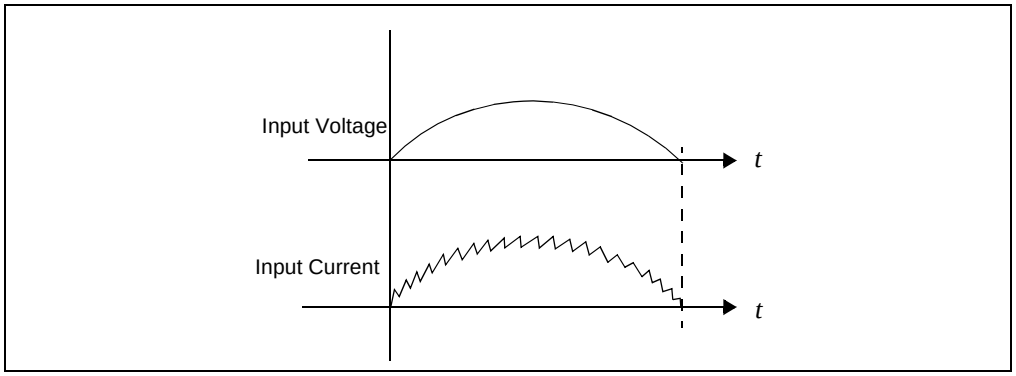


FIGURE 1-8: BOOST PFC INPUT CURRENT SHAPE



1.2.1.2.3 Buck/Boost PFC Circuit

In the Buck/Boost PFC circuit, the output DC voltage may be either less or greater than the input rectified voltage. High Power Factor can be achieved in this case. The switch (MOSFET) is rated to (VIN + VOUT). Figure 1-9 shows the circuit for the Buck/Boost PFC stage. Figure 1-10 shows the Boost PFC input current shape.

FIGURE 1-9: BUCK/BOOST PFC

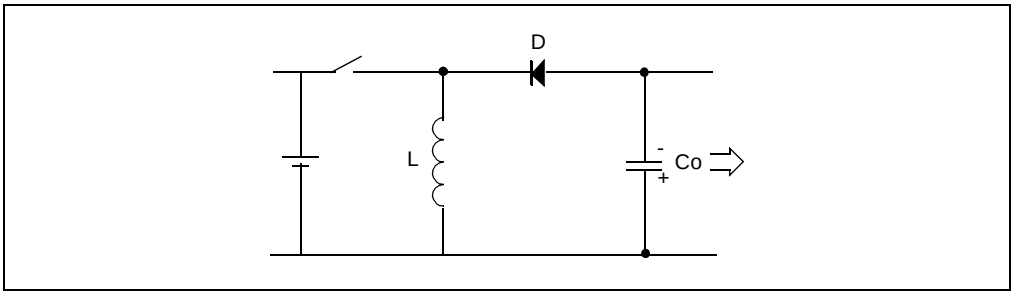
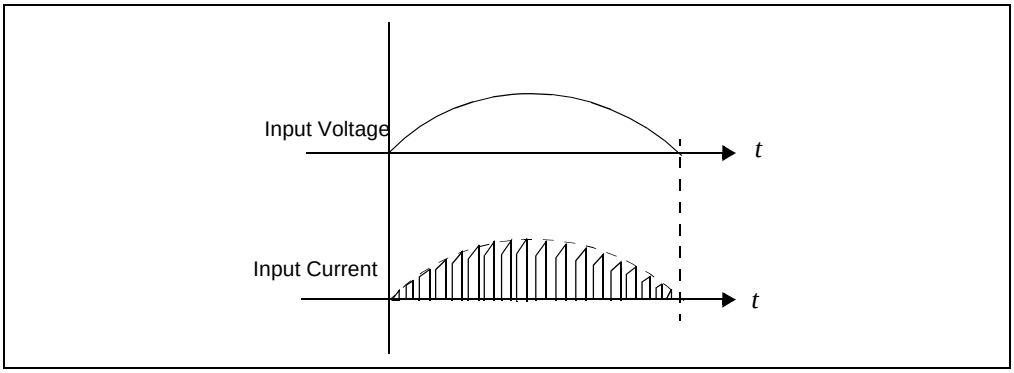


FIGURE 1-10: BUCK/BOOST PFC INPUT CURRENT SHAPE

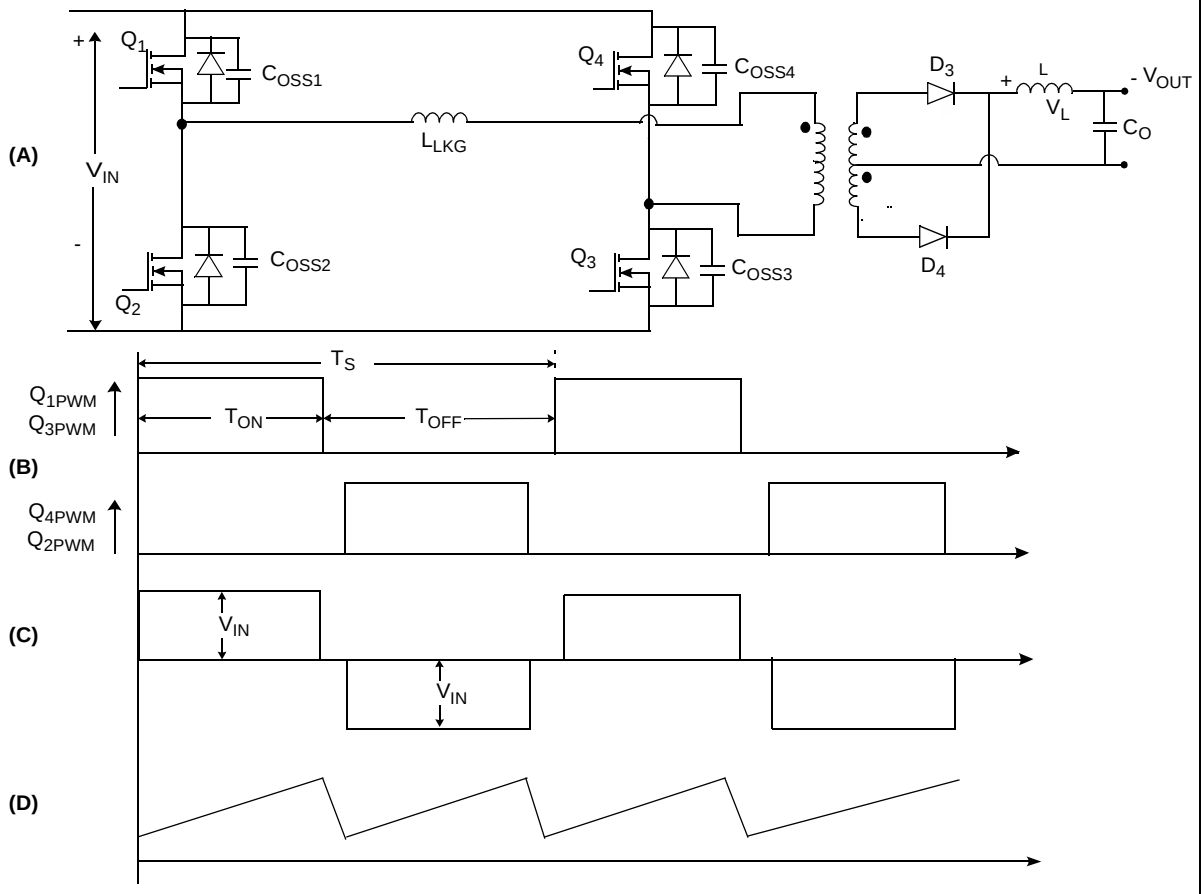


Regardless of the input line voltage and output load variations, input current drawn by the Buck converter and the Buck/Boost converter is always discontinuous. However, when the Boost converter operates in Continuous Conduction mode, the current drawn from the input voltage source is always continuous and smooth as shown in Figure 1-8. This feature makes the Boost converter an ideal choice for the Power Factor Correction (PFC) application. In PFC, the input current drawn by the converter should be continuous and smooth enough to meet Total Harmonic Distortion (THD) specifications for the input current (ITHD) such that it is close to unity. In addition, input current should follow the input sinusoidal voltage waveform to meet displacement factor such that it is close to unity.

1.2.2 Phase-Shift ZVT Converter

A Full-Bridge converter is a transformer isolated Buck converter. The basic schematic and switching waveform is shown in Figure 1-11. The transformer primary is connected between the two legs formed by switches Q1,Q2 and Q4,Q3. Switches Q1,Q2 and Q4, Q3 create a pulsating AC voltage at the transformer primary. The transformer is used to step down the pulsating primary voltage, as well as to provide isolation between the input voltage source and the output voltage V_{OUT}. A Full-Bridge converter configuration retains the voltage properties of the Half-Bridge topology, and the current properties of push-pull topology. The diagonal switch pairs, Q1,Q3 and Q4,Q2, are switched alternately at the selected switching period. Since the maximum voltage stress across any switch is V_{IN}, and with the complete utilization of magnetic core and copper, this combination makes the Full-Bridge converter an ideal choice for high input voltage, high-power range SMPS applications.

FIGURE 1-11: FULL-BRIDGE CONVERTER



(A) = Full-Bridge/Half-Bridge Phase-Shift ZVT converter
(B) = PWM gate pulse waveform for Full-Bridge switches
(C) = Voltage across the transformer primary
(D) = Output inductor and rectifier diode current

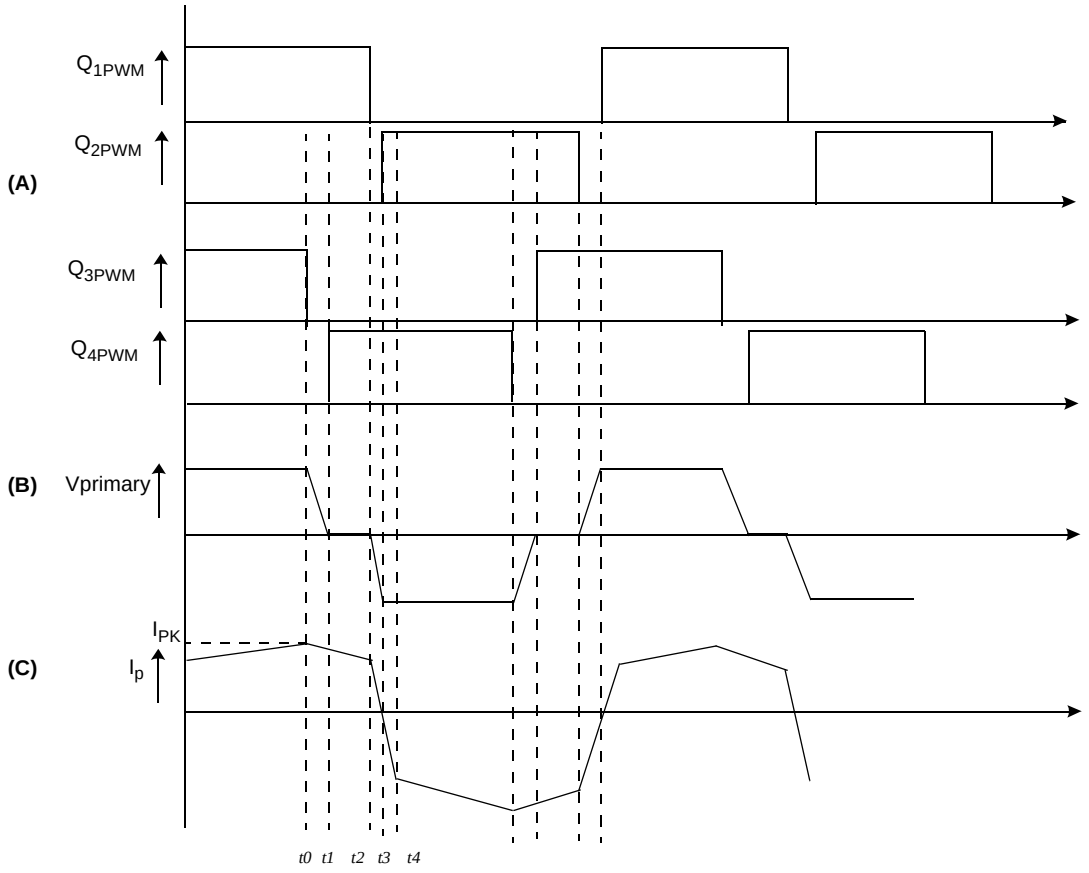
In the Full-Bridge converter, four switches are used, thereby increasing the amount of switching device loss. The conduction loss of a MOSFET can be reduced by using a MOSFET with a low $R_{DS(ON)}$ rating. Switching losses can be reduced by using Zero Voltage Transition (ZVT), Zero Current Switching (ZCS), or both techniques. At high power output and high input voltage, the ZVT technique is preferred for the MOSFET. In a Phase-Shift ZVT converter, the output is controlled by varying the phase of switch Q4 with respect to Q1.

In this topology, the parasitic output capacitor of the MOSFETs, and the leakage inductance of the switching transformer, are used as a resonant tank circuit to achieve zero voltage across the MOSFET at the turn-on transition. There are two major differences in the operation of a Phase-Shift ZVT and simple Full-Bridge topology. In a Phase-Shift ZVT converter, the gate drive of both diagonal switches is phase shifted. In addition, both halves of the bridge switch network are driven through the complementary gate pulse with a fixed 50% duty cycle. The phase difference between the two half-bridge switching network gate drives control the power flow from primary to secondary, which results in the effective duty cycle.

Power is transferred to the secondary only when the diagonal switches are ON. If the top or bottom switches of both legs are ON simultaneously, zero voltage is applied across the transformer primary. Therefore, no power is transferred to the secondary during this period. When the appropriate diagonal switch is turned OFF, primary current flows through the output capacitor of the respective MOSFETs causing switch drain voltage to move toward to the opposite input voltage rail. This creates zero voltage across the MOSFET to be turned ON next, which creates zero voltage switching when it turns ON. This is possible when enough circulating current is provided by the inductive storage energy to charge and discharge the output capacitor of the respective MOSFETs. Figure 1-12 shows the gate pulse required, and the voltage and current waveform across the switch and transformer.

The operation of the Phase-Shift ZVT can be divided into different time intervals. Assuming that the transformer was delivering the power to the load, the current flowing through primary is I_{PK}, and the diagonal switch Q1,Q3 was ON, at $t = t0$, the switch Q3 is turned OFF as shown in Figure 1-12.

FIGURE 1-12: REQUIRED GATE PULSES AND VOLTAGE AND CURRENT ACROSS PRIMARY



(A) = Gate pulse for all switches for Phase-Shift ZVT converter
(B) = Voltage across primary
(C) = Current across primary

1.2.2.1 TIME INTERVALS

- **Interval1: t0 < t < t1**

  Switch Q3 is turned OFF, beginning the resonant transition of the right leg. Primary current is maintained constant by the resonant inductor LLK. The primary current charges the output capacitor of switch Q3 (COSS3) to the input voltage VIN, which results in the output capacitance of Q4 (COSS4) being discharged to zero potential. This creates zero potential across switch Q4 prior to turn-on, resulting in zero voltage switching. During this transition period, the transformer primary voltage decreases from VIN to zero, and the primary no longer supplies power to the output. Inductive energy stored in the output inductor, and zero voltage across the primary, cause both output MOSFETs to share the load current equally.

- **Interval2: t1 < t < t2**

  After charging COSS3 to VIN, the primary current starts flowing through the body diode of Q4. Q4 can then be turned on any time after t1 and have a zero voltage turn-on transition.

- **Interval3: t2 < t < t3**

  At $t = t2$, Q1 was turned OFF and the primary was maintained by the resonant inductor LLK. In addition, at $t = t2$, IP is slightly less than the primary peak current IPK because of finite losses. The primary resonant current charges the output capacitor of switch Q1 (COSS1) to input voltage VIN, which discharges the output capacitor of Q2 (COSS2) to zero potential, thus preparing for zero voltage turn-on for switch Q2. During this transition, the primary current decays to zero. ZVS of the left leg switches depending on the energy stored in the resonant inductor, conduction losses in the primary switches and the losses in the transformer winding. Since the left leg transition depends on leakage energy stored in the transformer, it may require an external series inductor if the stored leakage energy is not enough for ZVS. When Q2 is then turned ON in the next interval, voltage VIN is applied across the primary in the reverse direction.

- **Interval: t3 < t < t4**

  The two diagonal switches Q4, Q2 are ON, applying full input voltage across the primary. During this period, the magnetizing current, plus the reflected secondary current into the primary, flows through the switch. The exact diagonal switch-on time depends on the input voltage, the transformer turns ratio and the output voltage. After the switch-on time period of the diagonal switch, Q4 is turned OFF.

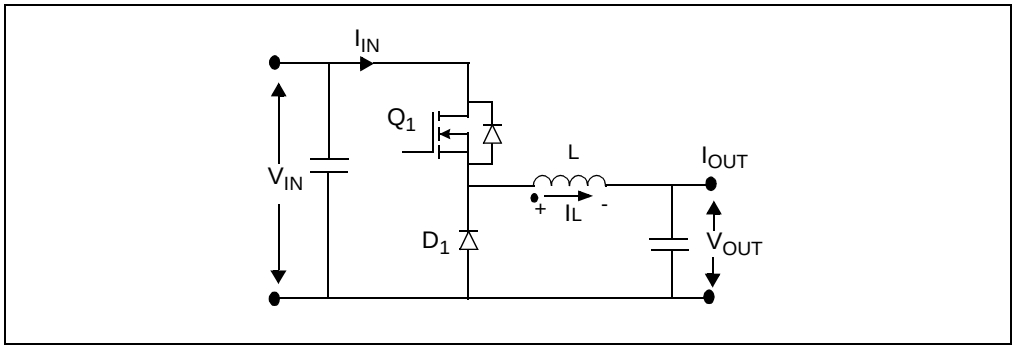
  One switching cycle is completed when the switch Q4 is turned OFF. The primary current charges COSS4 to a potential of input voltage VIN, and discharges COSS3 to zero potential, thereby enabling ZVS for switch Q3. The identical analysis is required for the next half cycle.

In the Phase-Shift ZVT converter shown in Figure 1-11, the maximum transition time occurs for the left leg at minimum load current and maximum input voltage, and minimum transition time occurs for the right leg at maximum load current and minimum input voltage. Therefore, to achieve ZVT for all switches, enough inductive energy must be stored to charge and discharge the output capacitance of the MOSFET in the specified allocated time. Energy stored in the inductor must be greater than the capacitive energy required for the transition. The MOSFET output capacitance varies as applied drain-to-source voltage varies. Thus, the output capacitance of the MOSFET should be multiplied by a factor of 4/3 to calculate the equivalent output capacitance.

1.2.3 Buck Converter Description and Background

A Buck converter, as its name implies, can only produce lower average output voltage than the input voltage. The basic schematic of a Buck converter is shown in Figure 1-13. The switching waveforms for a Buck converter are shown in Figure 1-14.

FIGURE 1-13: BUCK CONVERTER

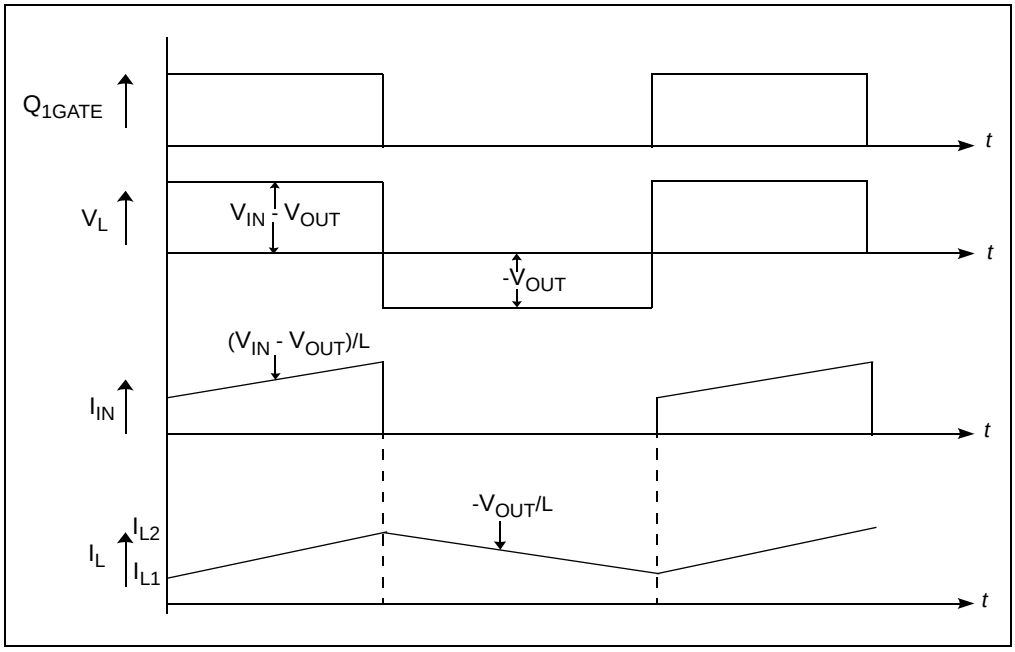


In a Buck converter, a switch (Q1) is placed in series with the input voltage source VIN. Input source VIN feeds the output through the switch and a low-pass filter, implemented with an inductor and a capacitor.

In a steady state of operation, when the switch is ON for a period of TON, the input provides energy to the output as well as to the inductor (L). During the TON period, the inductor current flows through the switch and the difference of voltages between VIN and VOUT is applied to the inductor in the forward direction, as shown in Figure 1-13. Therefore, the inductor current IL rises linearly from its present value IL1 to IL2.

During the TOFF period, when the switch is OFF, the inductor current continues to flow in the same direction as the stored energy within the inductor, which continues to supply the load current. Diode D1 completes the inductor current path during the Q1 OFF period (TOFF); thus, it is called a freewheeling diode. During the TOFF period, the output voltage VOUT is applied across the inductor in the reverse direction, as shown in Figure 1-14. Therefore, the inductor current decreases from its present value IL2 to IL1.

FIGURE 1-14: BUCK CONVERTER SWITCHING WAVEFORM



The inductor current is continuous and never reaches zero during one switching period (TS); therefore, this mode of operation is known as Continuous Conduction mode. In Continuous Conduction mode, the relation between the output and input voltage is given by Equation 1-1. The duty cycle is given by Equation 1-2.

EQUATION 1-1:

$$V_{OUT} = D \cdot V_{IN}$$

where D is the duty cycle

EQUATION 1-2:

$$D = \frac{t_{on}}{T_S}$$

where t_{on} is the ON time and T_S is the switching time period

When the output current requirement is high, the excessive power loss inside freewheeling diode D1 limits the minimum output voltage that can be achieved. To reduce the loss at high current, and to achieve lower output voltage, the freewheeling diode is replaced by a MOSFET with a very low ON state resistance ($R_{DS(ON)}$). This MOSFET is turned on and off synchronously with the Buck MOSFET. Therefore, this topology is known as a Synchronous Buck converter. A gate drive signal, which is the complement of the Buck switch gate drive signal, is required for this synchronous MOSFET.

A MOSFET can conduct in either direction; which means the synchronous MOSFET should be turned off immediately if the current in the inductor reaches zero because of a light load. Otherwise, the direction of the inductor current will reverse (after reaching zero) because of the output LC resonance. In such a scenario, the synchronous MOSFET acts as a load to the output capacitor, and dissipates energy in the $R_{DS(ON)}$ of the MOSFET, resulting in an increase in power loss during the discontinuous mode of operation (inductor current reaches zero in one switching cycle). This may happen if the Buck converter inductor is designed for a medium load, but needs to operate at no load and/or a light load. In this case, the output voltage may fall below the regulation limit if the synchronous MOSFET is not switched off immediately after the inductor reaches zero.

1.3 MULTI-PHASE SYNCHRONOUS BUCK CONVERTER

If the load current requirement is more than 35-40 amps, more than one converter is connected in parallel to deliver the load. To optimize the input and output capacitors, all the parallel converters operate on the same time base and each converter starts switching after a fixed time/phase from the previous one. This type of converter is called a Multi-Phase Synchronous Buck converter, which is shown in Figure 1-15. Figure 1-16 shows gate pulse timing relation of each leg and the input current drawn by the converter. The fixed time/phase is given by Time period/n (or 360/n), where “n” is the number of the converters connected in parallel.

The design of input and output capacitors is based on the switching frequency of each converter multiplied by the number of parallel converters. The ripple current seen by the output capacitor reduces by “n” times. As shown in Figure 1-16, the input current drawn by a Multi-Phase Synchronous Buck converter is continuous, with less ripple current as compared to a single converter. Therefore, a smaller input capacitor meets the design requirement in the case of a Multi-Phase Synchronous Buck converter.

FIGURE 1-15: MULTI-PHASE SYNCHRONOUS BUCK CONVERTER

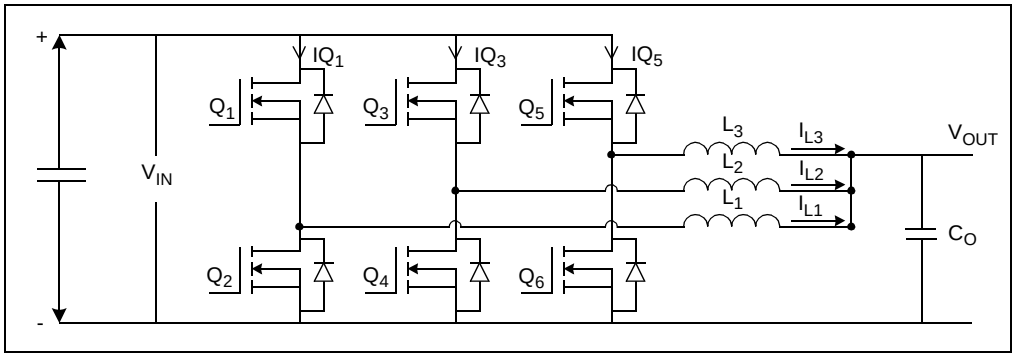
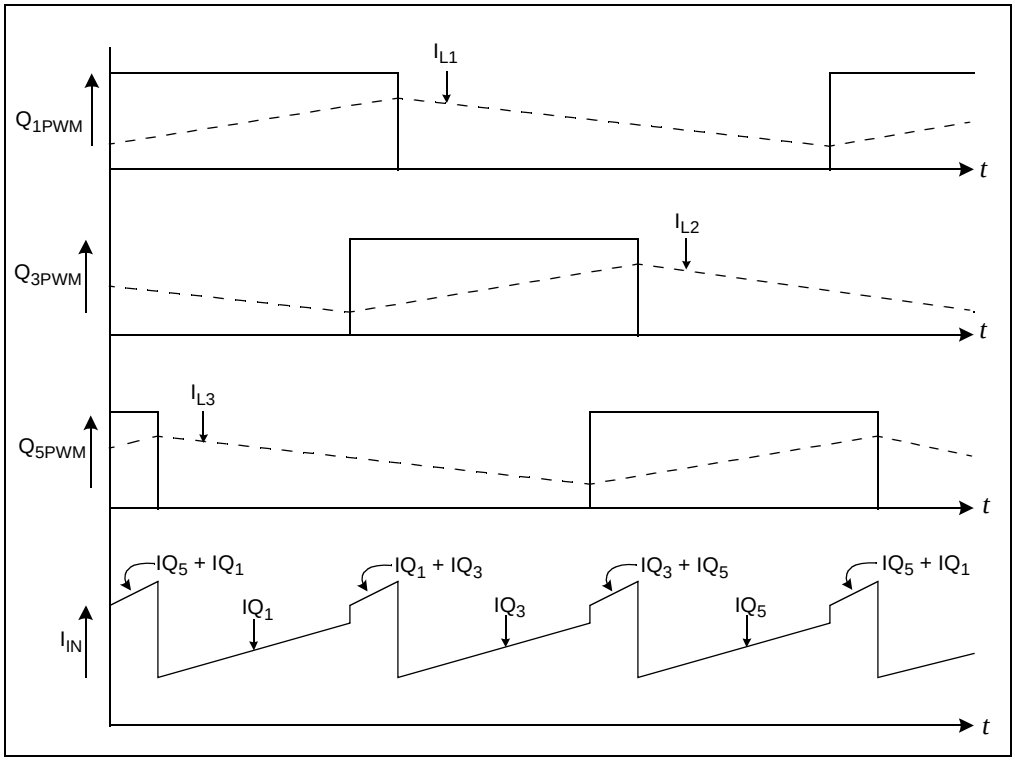


FIGURE 1-16: SWITCHING WAVEFORM OF SYNCHRONOUS BUCK CONVERTER

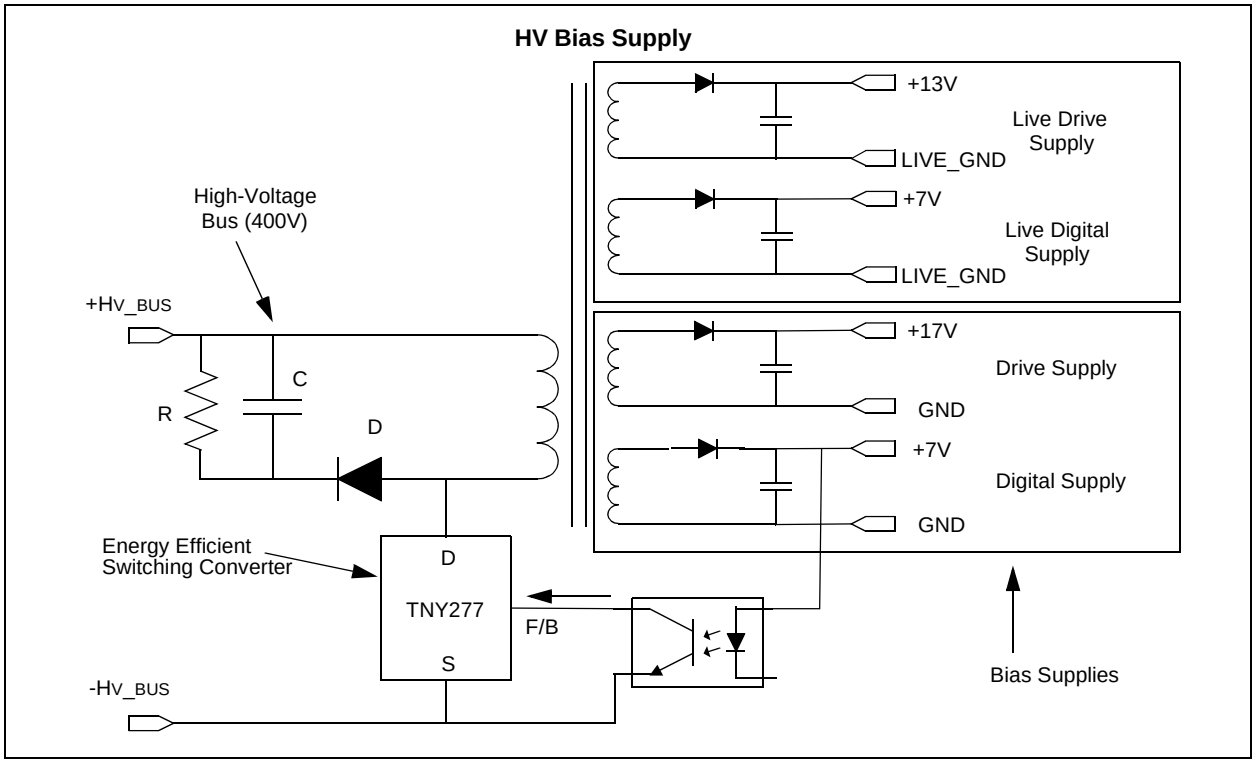


1.3.1 Auxiliary Supply Description

The auxiliary power supply is based on the flyback topology, where it generates a voltage source for the control circuitry and MOSFET drivers on both sides of the isolation boundary. The multiple output flyback converter is controlled by a TNY277G switch; the block diagram is shown in Figure 1-17. The auxiliary power supply generates four isolated outputs, where on each side of the isolation barrier, the auxiliary transformer will generate a voltage source for the MOSFET drivers and a voltage source for the control circuitry.

A flyback converter is a transformer-isolated converter based on the basic Buck topology. In a flyback converter, a switch is connected in series with the transformer primary. The transformer is used to store energy during the ON period of the switch, and provides isolation between the input voltage source V_{IN} and the output voltage V_{OUT}. During the T_{OFF} period, the energy stored in the primary of the flyback transformer transfers to secondary through the flyback action. This stored energy provides energy to the load, and charges the output capacitor. Since the magnetizing current in the transformer cannot change instantaneously when the switch is turned OFF, the primary current transfers to the secondary, and the amplitude of the secondary current will be the product of the primary current and the transformer turns ratio.

FIGURE 1-17: AUXILIARY POWER SUPPLY BLOCK DIAGRAM



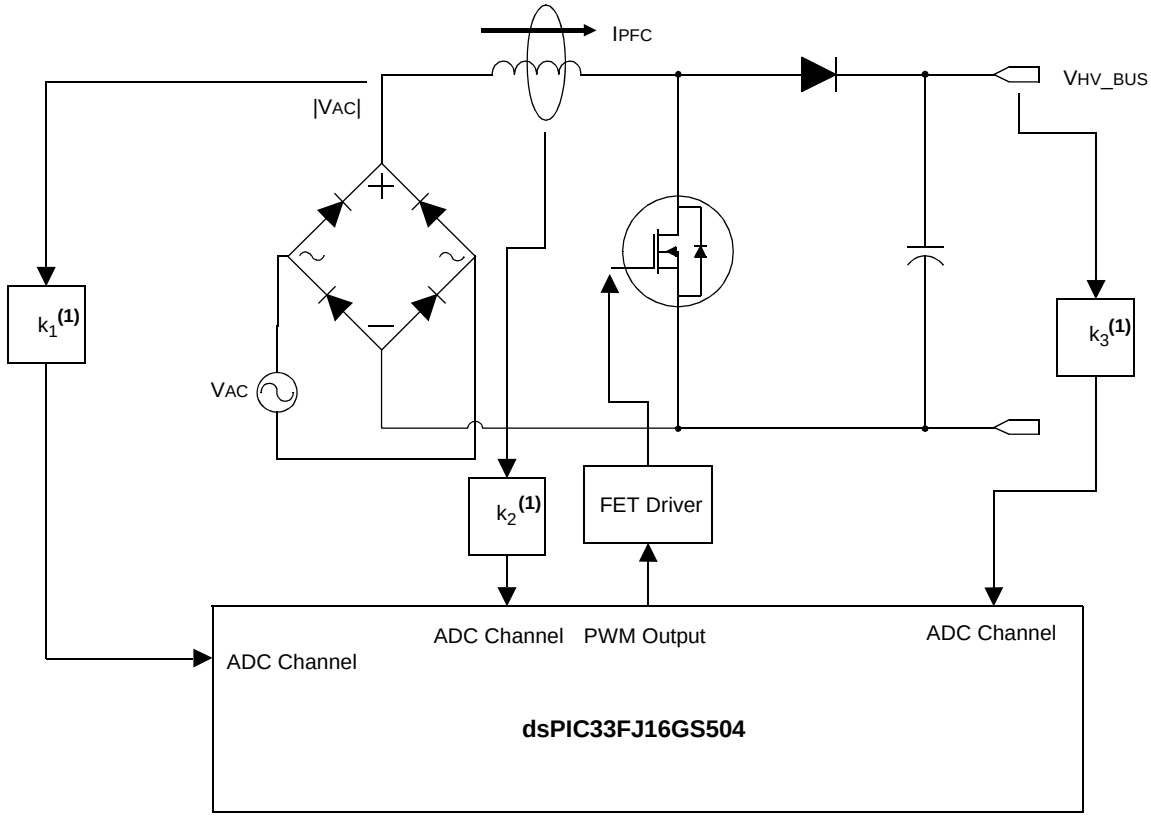
At the end of the ON period, when the switch is turned OFF, there is no current path to dissipate the stored leakage energy in the magnetic core of the flyback transformer. There are many ways to dissipate this leakage energy. One such method is shown in Figure 1-17 as a snubber circuit consisting of D, R, and C. In this method, the leakage flux stored inside the magnetic core induces positive voltage at the non-dot end primary winding, which forward-biases diode D and provides the path to the leakage energy stored in the core, and clamps the primary winding voltage to a safe value. Because of the presence of the secondary reflected voltage on the primary winding and the leakage stored energy in the transformer core, the maximum voltage stress VDS of the switch is approximately 1.6 times the input voltage (i.e., 400•1.6 = 660V).

1.4 LISTING OF I/O SIGNALS FOR EACH BLOCK, TYPE OF SIGNAL AND EXPECTED SIGNAL LEVELS

1.4.1 PFC Boost Converter

As indicated in the block diagram in Figure 1-18, three input signals are required to implement the control algorithm. The only output from the dsPIC DSC device is firing pulses to the Boost converter switch to control the nominal voltage on the DC bus in addition to presenting a resistive load to the AC line. Table 1-1 shows the dsPIC DSC resources used by the PFC application.

FIGURE 1-18: RESOURCES REQUIRED FOR DIGITAL PFC



Note 1: K_1, K_2 and K_3 are feedback gain circuits. See **A.3 "SMPS AC/DC Reference Design Schematics"** for detailed schematics.

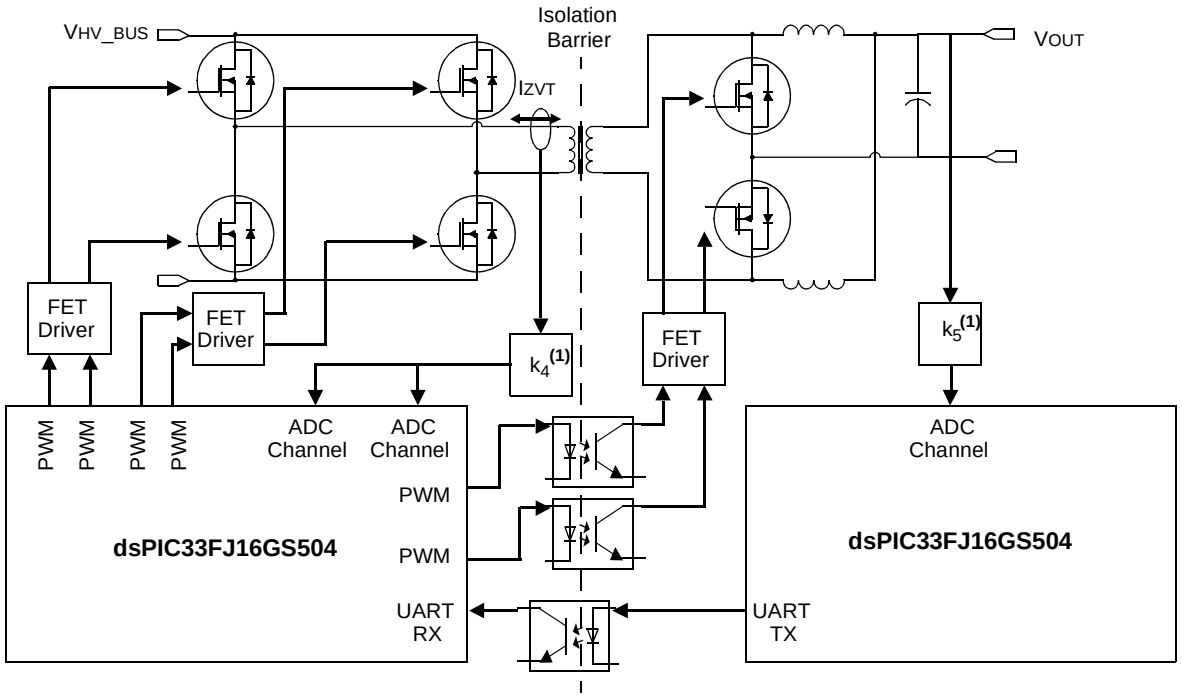
TABLE 1-1: RESOURCES REQUIRED FOR DIGITAL PFC

Description	Type of Signal	dsPIC® DSC Resources Used	Expected Signal Level
Output Voltage (VHV_BUS)	Analog	AN5	3.01V (nominal)
PFC Current (IPFC)	Analog	AN4	2.5V (maximum)
AC Input Voltage (VAC)	Analog	AN3	1.9V (maximum)
PFC Gate Drive	PFC Drive Output, Digital	PWM4L	—

1.4.2 Phase-Shift ZVT Converter

As indicated in the block diagram in Figure 1-19, three input signals are required to implement the control algorithm. The only outputs from the dsPIC DSC device are firing pulses to the Full-Bridge Phase-Shift ZVT and synchronous MOSFETs to control the nominal voltage on VOUT.

FIGURE 1-19: RESOURCES REQUIRED FOR DIGITAL PHASE-SHIFT ZVT CONVERTER



Note 1: K_4 and K_5 are feedback gain circuits. See **A.3 "SMPS AC/DC Reference Design Schematics"** for detailed schematics.

Table 1-2 shows the dsPIC DSC resources used by Phase-Shift ZVT application.

TABLE 1-2: RESOURCES REQUIRED FOR DIGITAL PHASE-SHIFT ZVT

Description	Type of Signal	dsPIC® DSC Resources Used	Expected Signal Level
ZVT CURRENT 1 (IZVT1)	Analog	AN0	1.5V (maximum)
ZVT CURRENT 2 (IZVT2)	Analog	AN2	1.5V (maximum)
Voltage Sense (VOUT)	Analog	AN5 (secondary side)	2.79V (maximum)
ZVT Gate Drive	Full-Bridge Drive Outputs, Digital	PWM1H, PWM1L, PWM2H, PWM2L	—
Synchronous Rectifier Gate Drive	Sync FET Drive Outputs, Digital	PWM3H, PWM3L	—

Table 1-3 shows the common resources used on the Primary side.

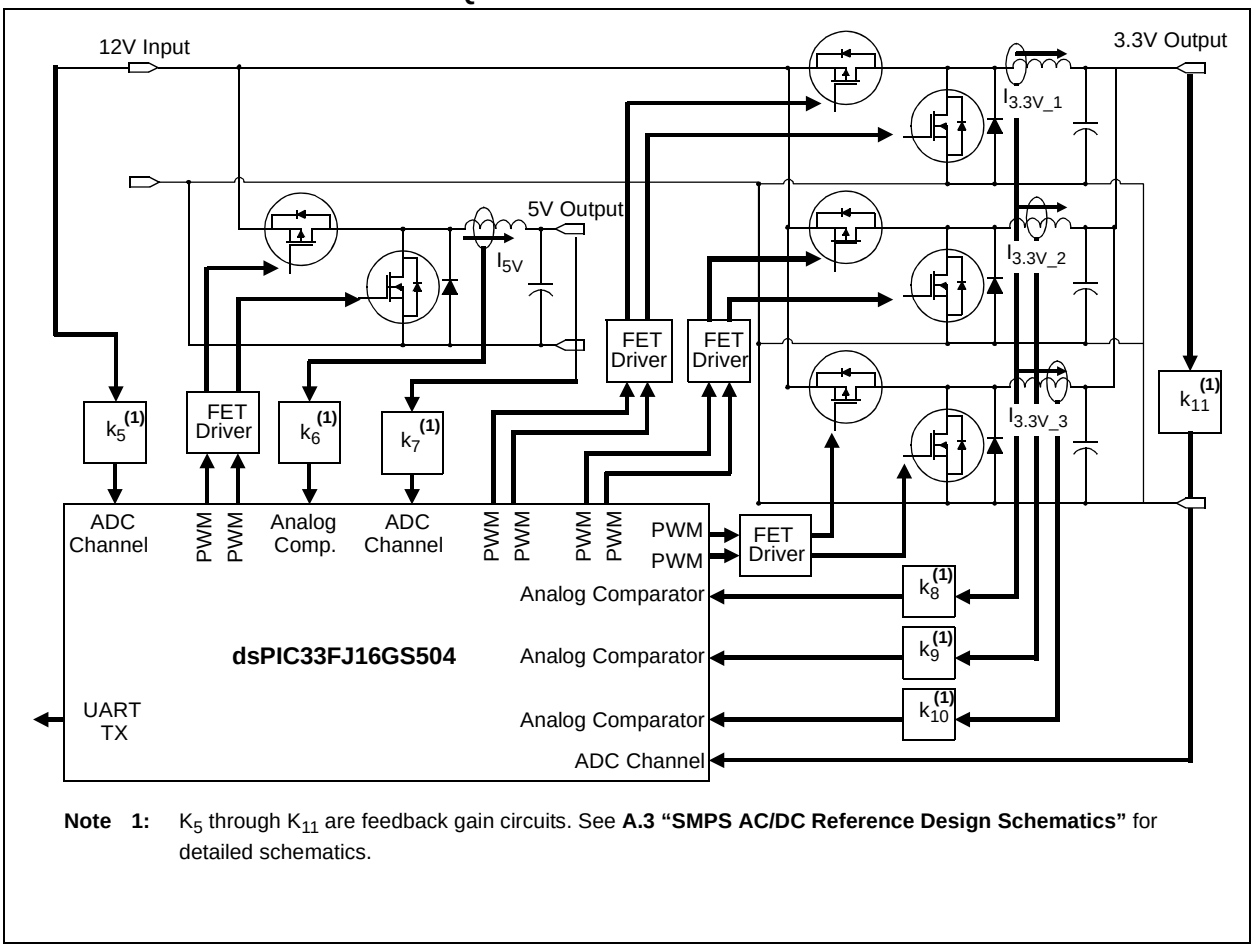
TABLE 1-3: PRIMARY COMMON RESOURCES

Signal Name	Type of Signal	dsPIC® DSC Resources Used	Expected Signal Level
Live_MCLR	Digital	$\overline{MCLR}$	—
Live_PGC	Digital	PGC	—
Live_PGD	Digital	PGD	—
Live_Fault	Digital	RC6	—
Live_RS232_TX	Digital	UART1 Transmit	—
Live_RS232_RX	Digital	UART1 Receive	—
Live_Temp_Sense	Analog	AN10	1.4V

1.4.3 Secondary Side Synchronous Buck Converters

Figure 1-20 shows the input signals required to implement the control algorithms for the synchronous Buck converters. The output from the dsPIC DSC device is firing pulses to the Multi-Phase as well as Single-Phase Synchronous Buck converters.

FIGURE 1-20: RESOURCES REQUIRED FOR DIGITAL SYNCHRONOUS BUCK CONVERTERS



Note 1: K_5 through K_{11} are feedback gain circuits. See **A.3 "SMPS AC/DC Reference Design Schematics"** for detailed schematics.

Table 1-4 shows the dsPIC DSC resources used by Multi-Phase as well as Single-Phase Synchronous Buck converters.

TABLE 1-4: RESOURCES REQUIRED FOR SECONDARY SIDE SYNCHRONOUS BUCK CONVERTERS

Description/Signal Name	Type of Signal	dsPIC® DSC Resources Used	Expected Signal Level
5V Buck Current	Analog	AN0, CMP1A	1.25V (maximum)
5V Buck Output	Analog	AN1	2.7V (nominal)
3.3V Buck Current 1	Analog	AN2, CMP2A	1V (maximum)
3.3V Buck Current 2	Analog	AN4, CMP3A	1V (maximum)
3.3V Buck Current 3	Analog	AN6, CMP4A	1V (maximum)
3.3V Buck Output	Analog	AN3	1.65V (nominal)
5V Buck Gate Drive	Single-Phase Synchronous Buck Drive	PWM4H, PWM4L	—
3.3V Buck Gate Drive	Multi-Phase Synchronous Buck Drive	PWM1H, PWM1L, PWM2H, PWM2L, PWM3H, PWM3L,	—
12V Bus Sense	Analog	AN5	2.79V
12V Digital Feedback	Digital	UART1 Transmit	—
RS232_RX	Digital	UART1 Receive	—
Temperature Sense	Analog	AN8	1.4V
$\overline{\text{MCLR}}$	Digital	$\overline{\text{MCLR}}$	—
PGC	Digital	PGC	—
PGD	Digital	PGD	—
Fault_Reset	Digital	RC6	—

Chapter 2. Hardware Design

This chapter provides a functional overview of the SMPS AC/DC Reference Design and identifies the major hardware components. Topics covered include:

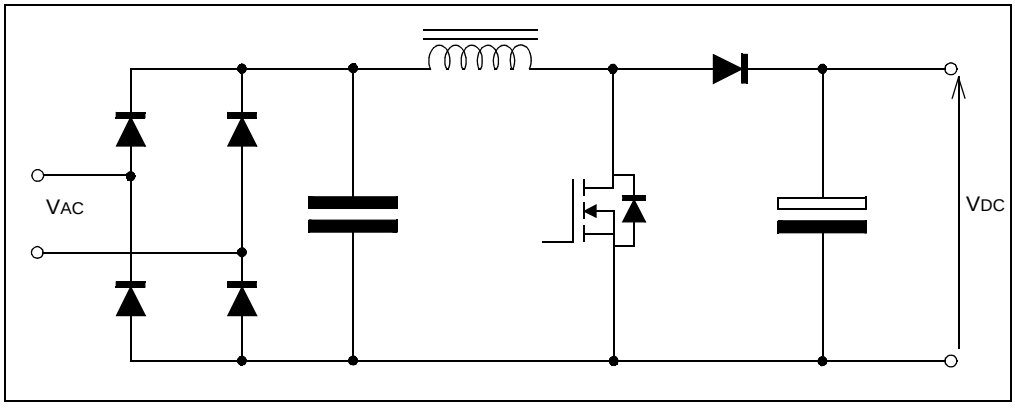
- PFC Boost Converter
- Full-Bridge ZVT Converter
- Single-Phase Synchronous Buck Converter
- Three-Phase Synchronous Buck Converter
- Auxiliary Power Supply

2.1 PFC BOOST CONVERTER

The conventional single-phase power factor correction circuit is a standard Boost converter topology operating from the full wave rectified mains input, as shown in Figure 2-1.

The converter controller has an inner current control loop and outer voltage control loop. The current reference waveform is the input rectified mains voltage, so that the resultant current drawn from the mains is essentially sinusoidal and in-phase with the mains voltage. The amplitude of the current is controlled by the duty cycle of the fixed frequency PWM of the MOSFET, and is controlled by the PWM reference, which is the product of the current reference and the output of the DC link voltage error amplifier. Refer to **Chapter 1. "Introduction"** for details on the operation of this converter.

FIGURE 2-1: PFC POWER CONVERTER



EQUATION 2-1:

$$D(t) = 1 - \frac{V_{ac}(t)}{V_{dc}}$$

EQUATION 2-2:

$$THD = 100\frac{\sqrt{\tilde{I}_{ac}^2 - \tilde{I}_1^2}}{\tilde{I}_1}$$

2.1.1 Power-Train Design

The target specification for the PFC converter is as follows:

- Input voltage, VIN = 85-265 Vrms
- Input frequency, f_{in} = 45-65 Hz
- Switching frequency, f_{sw} = 125 kHz
- Maximum Output voltage, VOUT = 420 VDC
- Maximum Output power, POUT = 450 W
- Current THD < 5%

EMC standards for conducted, radiated and line current harmonics:

- FCC Class B
- EN55022 (CISPR 22) Class B
- EN61000-3-2 A14 Class A
- EN61000-3-3
- IEEE519

2.1.1.1 MOSFETS AND GATE DRIVE

MOSFETs are the preferred technology for the Boost converter power switch because of the high operating frequency. The rms current in the MOSFET switch can be approximated using Equation 2-3.

EQUATION 2-3:

$$\tilde{i}_{mos} = \frac{P_o}{V_{ac}\sqrt{2}}\sqrt{2 - \frac{16V_{ac}\sqrt{2}}{3\pi V_{dc}}}$$

$$P_{sw} = \tfrac{1}{2} C_{oss} V_{dc}^2 f_{sw}$$

The maximum rms current occurs at minimum mains voltage, so the maximum normal operating MOSFET current is 4.6 Arms. Therefore, two TO-220 Infineon CoolMOS™ SPP11N60CFD 500V, 0.44Ω MOSFETs are connected in parallel, with each dissipating 2.3W of conduction loss. The MOSFET output capacitance is 390 pF so the switching loss is estimated at about 0.4W each. The actual loss in practice will be layout dependent and will probably be a factor of 2 higher, but still low enough to achieve high system efficiency.

The gate drive circuitry is a low-side Microchip TC1412N gate-drive IC, which drives the MOSFET gates directly. A single dsPIC DSC PWM module pin interfaces with the gate-drive IC via an inverting open-collector transistor stage which provides immunity against noise voltage differences between the Boost converter common and dsPIC DSC signal common (ground bounce).

2.1.1.2 OUTPUT DIODE

The output diode must be rated for the mean output current, which is given by Equation 2-4.

EQUATION 2-4:

$$\bar{i}_{diode} = \frac{P_o}{V_{dc}}$$

In this design, the diode must be rated for 1.2A, so a STMicroelectronics STTH5R06D 600V, 5A TO-220 ultra-fast high-voltage rectifier has been selected. The typical forward voltage drop at high junction temperature is 1.4V, which means that the device will run cool since the dissipation is only 1.7 Watts. There will be additional switching losses due to the high switching frequency and diode recovery characteristics. For a lower cost solution, a smaller axial diode may be used. Alternatively, if switching losses are an issue, then the recently introduced SiC Schottky diode would be an attractive option.

2.1.1.3 PFC CHOKE

The target THD of the input current is 5%, which means the non-fundamental (50 Hz nominal) rms current component must be only 1% of input rms current. This component is the high-frequency ripple current in the Boost inductor, and is dependent on the inductance. If it is assumed that, on average, the duty cycle is 0.5, the ripple current rms of a triangular waveform is given by Equation 2-5.

EQUATION 2-5:

$$I_{rms} = \sqrt{\frac{I_{pk-pk}^2}{12}}$$

Therefore, for a 5.3 Arms input current, we can only allow a maximum of 0.2A peak-to-peak, which will entail a large inductor size. However, the high frequency capacitor placed across the output terminals of the bridge rectifier will shunt-off most of the high frequency current so that a larger component of ripple can be tolerated in a smaller inductor. Note that too large a capacitance will cause distortion in the current waveform, so a design compromise must be reached. The inductor current peak-to-peak ripple in a PFC Boost converter varies over the whole mains cycle and depends on the input voltage, as shown in Equation 2-6.

EQUATION 2-6:

$$i_{ripple} = \frac{D\hat{V}_{ac}}{Lf_{sw}}$$

However, the absolute maximum value is independent of input voltage and is calculated from Equation 2-7.

EQUATION 2-7:

$$\hat{i}_{ripple} = \frac{V_{dc}}{4Lf_{sw}}$$

In this design, the ripple current is chosen to be 25% of the minimum voltage peak mains current; therefore, inductance of about 400 µH is required. The Boost choke uses a Kool Mu 77548 core, which has an outside diameter of 33 mm. The A_L value for this core is 127. A single layer of 58 turns of 0.9 mm (19 AWG) enameled copper fits on the core giving an unsaturated inductance of 427 µH. From the Magnetics Inc. published wire-core tables, this results in a predicted winding resistance of 77 mΩ at 100ºC. The variation of ripple current for a selection of input voltages is shown in Figure 2-2 and Figure 2-3.

The core loss can be roughly estimated from the mean flux density over a complete mains cycle. The worst case condition occurs at roughly 180 Vrms, where the mean flux density is 180 mT.

FIGURE 2-2: INPUT VOLTAGE RIPPLE CURRENT VARIATION

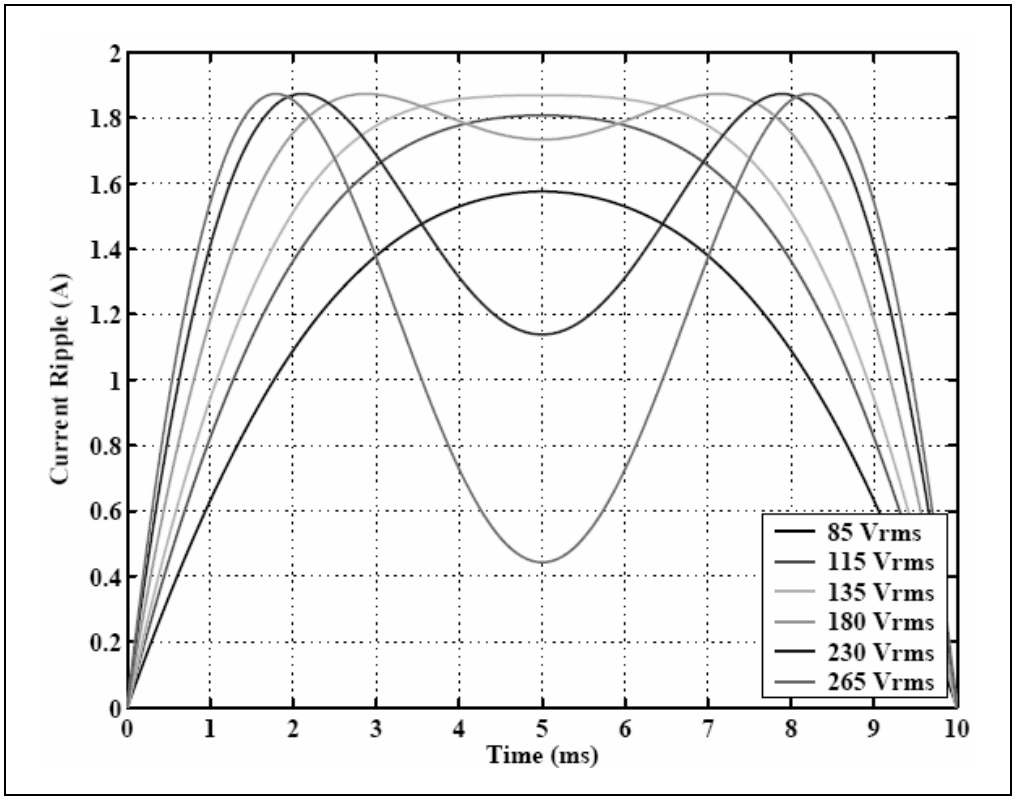
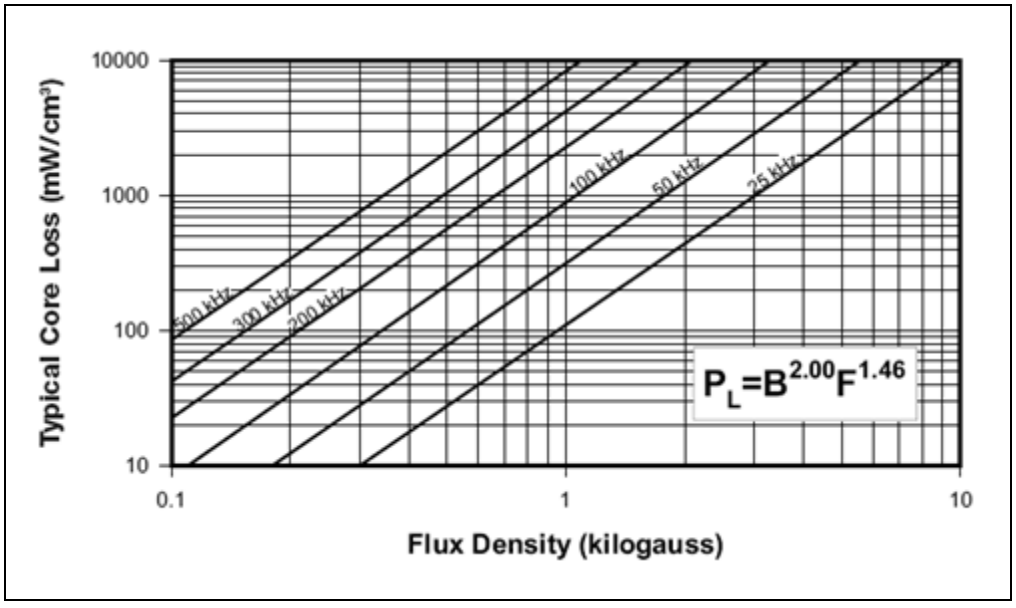


FIGURE 2-3: CORE LOSSES FOR PFC CHOKE



2.1.1.4 PFC OUTPUT CAPACITOR

The PFC output capacitor provides bulk capacitance on the output of the PFC Boost converter and smooths the DC voltage input to the ZVT Full-Bridge converter. The size of the capacitor is dictated by the hold-up requirements of the SMPS, its AC ripple current and thermal lifetime under normal operating conditions.

The capacitance must be high enough to maintain the PFC output voltage within acceptable bounds under normal peak power operating conditions and when a mains brown-out occurs. The required hold-up time, t_{hold}, at the minimum mains frequency is 22 ms, therefore the conditions of Equation 2-8 must be met.

EQUATION 2-8:

$$C > \frac{2t_{hold}P_o}{\left(V_{dc}^2 - V_{dc(\min)}^2\right)}$$

For a minimum DC link voltage of 300V, a 330 µF is required. The actual capacitor selected is a Panasonic EET-ED2W331EA 35 x 40 mm electrolytic capacitor rated to 450 VDC and 105ºC. The ESR at 20 kHz is 0.181Ω, and the maximum ripple current rating at 105ºC is 2.64 Arms.

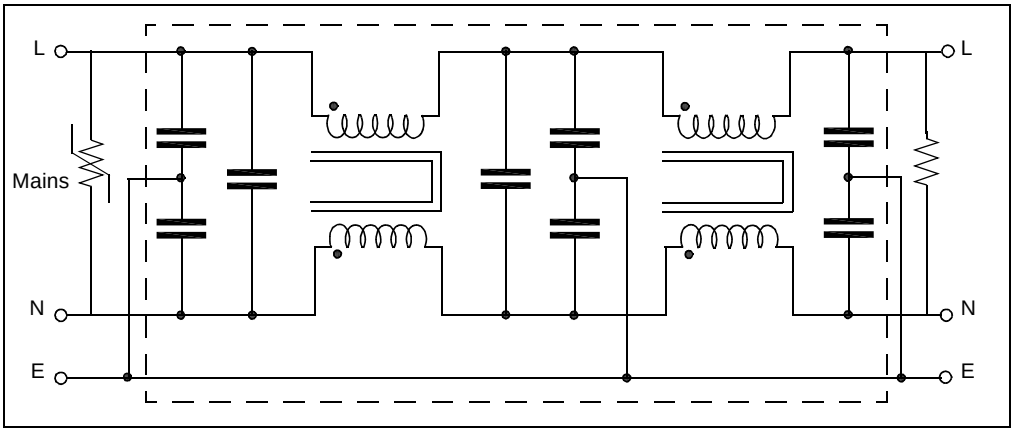
2.1.1.5 EMI FILTER

The SMPS AC/DC Reference Design has been designed to meet international standards for conducted EMC. The EMI filter between the mains input terminals and the PFC is a two-stage design because of the high switching frequency of the different stages in the SMPS. The circuit is shown in Figure 2-4. The two common-mode chokes are rated to 6 Arms, and the 2.2 mH inductance forms a filter with the capacitors to Earth Ground for common-mode noise. The leakage inductance of the chokes together with the capacitors across the live and neutral terminals, filter the differential-mode noise.

The six capacitors connected to Earth Ground are 2.2 nF Y2-class capacitors meeting the CATII overvoltage category. The two X2-class capacitors are 220 nF. A transient spike voltage protection MOV is also fitted across the mains input, and a 470 kΩ discharging resistor is fitted across the input to the SMPS to ensure that the filter capacitors discharge within one second.

Note:	The EMI/EMC filter value has been chosen based on switching frequencies and expected noise levels in the system. This value may be changed based on the final test results of EMI/EMC.

FIGURE 2-4: EMI FILTER



2.2 FULL-BRIDGE ZVT CONVERTER

The main power circuit for a ZVT Full-Bridge converter is shown in Figure 2-5. It is a standard Full-Bridge converter, but with additional series resonant inductance, which limits the rise rate of current at switching transitions and can eliminate turn-off switching power dissipation in the MOSFETs. The stray leakage inductance of the transformer forms part of the series resonant inductor and, in this particular design, is large enough to ensure quasi-resonant operation over 80% of the operating power range without the need for an additional inductor. The secondary-side high-frequency rectification is normally done by using ultrafast recovery rectifiers or Schottky diodes. Alternatively, lower loss rectification can be achieved by using MOSFETs operating as synchronous rectifiers with primary-side commutation control, and this is the preferred solution in this reference design.

ZVT operation occurs when the stored energy in the inductor is transferred to the capacitor in parallel with the MOSFET. In this design, the stray output capacitance of the MOSFET is large enough to not require additional capacitors in parallel. From Reference 3 (see **Appendix C. "References"**), the equation relating energy in the MOSFET output capacitance and the series inductance for ZVT operation is given by Equation 2-9.

EQUATION 2-9:

$$\frac{1}{2}L_R I_{pri}^2 \geq \frac{4}{3}C_R V_{in}^2$$

This ensures that there is more than enough energy to charge the MOSFET output capacitance and maintain ZVT operation. Note that at low output power, there will be far less energy stored in the resonant inductance so ZVT operation will be lost. The inductor is therefore selected based on the minimum operating output power for ZVT switching.

The modulation control scheme required for ZVT operation of a Full-Bridge converter is phase-shifted PWM. The ideal power stage waveforms for the circuit are shown in Figure 2-6. The ZVT transition in the switch is short in comparison with the primary current transition time. This time, Δt, is dictated by the resonant inductance, L_R, which is given by Equation 2-10.

EQUATION 2-10:

$$\Delta t = 2\frac{L_R I_{pri}}{V_{in}}$$

The control duty cycle is limited in a ZVT due to the time taken for the current to rise/fall during switching transitions. The maximum duty cycle, D_{max}, is achievable under the ZVT operating conditions given by Equation 2-11.

EQUATION 2-11:

$$D_{\max} = 1 - \frac{2\Delta t}{T}$$

The transformer turns ratio, n, for the current doubling synchronous rectifier topology can then be selected for the required operating input and output voltages using the following ideal relationship shown in Equation 2-12.

EQUATION 2-12:

$$n = D_{\max} \frac{V_{in}}{2V_o}$$

The previous equations governing the ZVT operation and resonant circuit component selection are also dependent on the peak primary current. If the output inductor magnetizing current is ignored, the primary peak current is given by Equation 2-13.

EQUATION 2-13:

$$I_{pri} = \frac{I_o V_{in}}{n^2 V_o}$$

FIGURE 2-5: ZVT FULL-BRIDGE POWER CONVERTER WITH SYNCHRONOUS RECTIFICATION

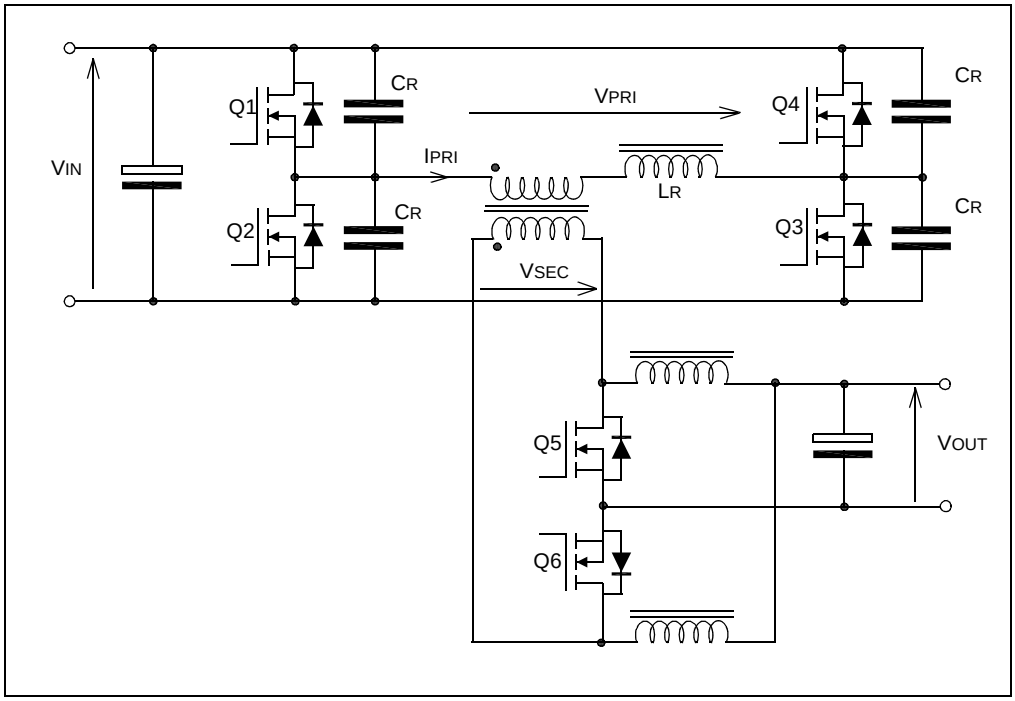
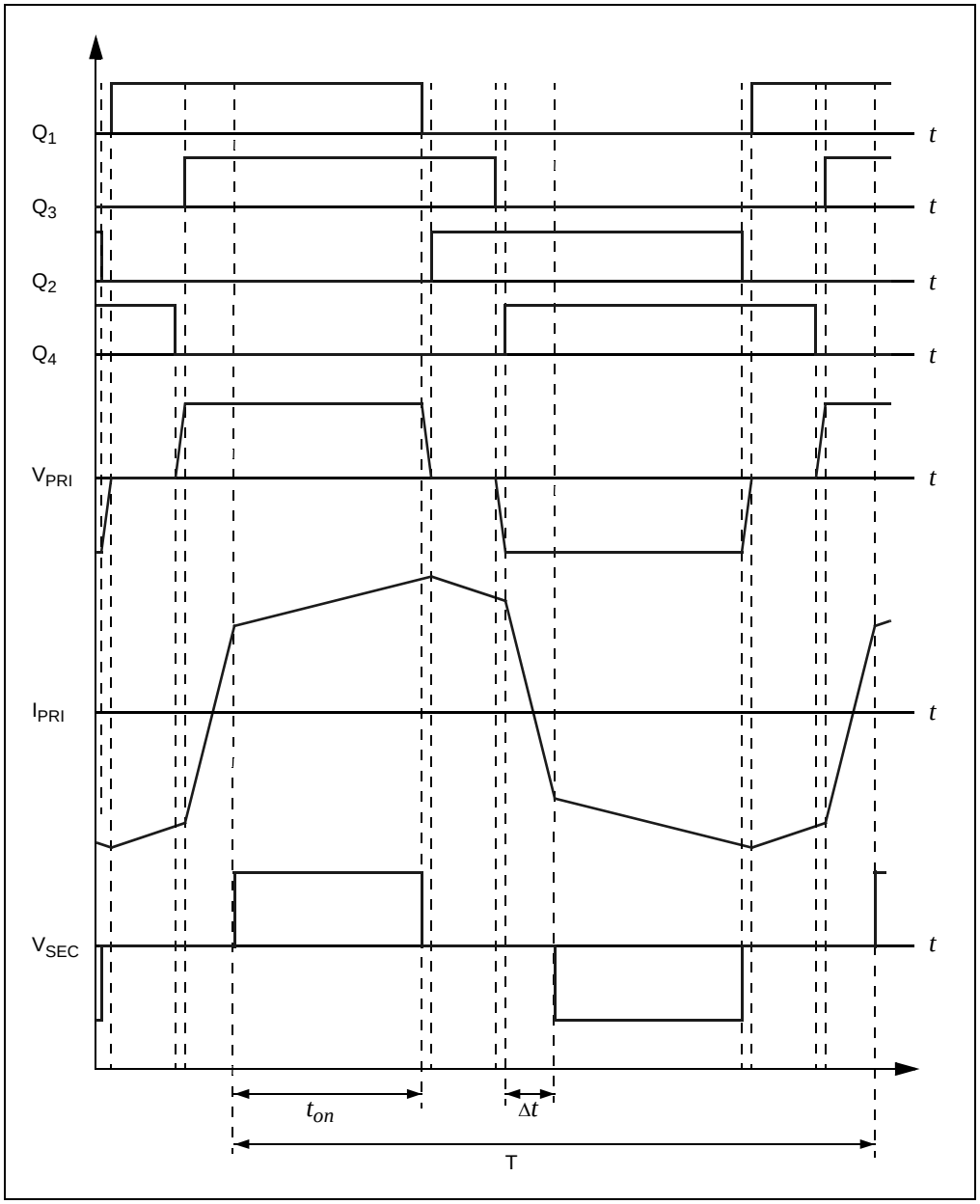


FIGURE 2-6: ZVT WAVEFORMS



2.2.1 Full-Bridge ZVT Power-Train Design

The target specification for the ZVT Full-Bridge converter is as follows:

- Input voltage, VIN = 390-420V
- Switching frequency, f_{sw} = 250 kHz
- Maximum output voltage, VOUT = 12V
- Maximum output current, IOUT = 33A

2.2.1.1 MOSFETS AND GATE DRIVE

Care must be taken when selecting the MOSFET switch for the ZVT Full-Bridge since there are potential failure modes associated with the diode characteristic and timing control at light loads (see Reference 4 in **Appendix C. "References"**). For this reference design, an Infineon CoolMOS CFD device has been selected because of its optimized diode characteristic. The SPA11N60CFD is a 600V, 0.44Ω MOSFET in a TO-220 package, and is a good compromise between cost and efficiency for this output power rating. The output capacitance, COSS, is 45 pF and will form the resonant capacitor for ZVT operation.

Gate driving is typically achieved with either a proprietary high-side and low-side high-voltage driver IC, or using a small transformer. These circuit techniques provide level-shifting of the dsPIC DSC gate firing signals. Adequate voltage creepage and clearance distances are maintained in the layout. Given the high switching frequency in this application, the transformer isolated gate drive approach has been adopted. This is because of thermal concerns in standard gate driver ICs, although there are potential candidates from a number of manufacturers available on the market.

A single drive transformer with two secondary windings manufactured by Sirio Elettronica is used for each half-limb, and the turn-on switching time is controlled by a single resistor in each MOSFET gate. Turn-off is much faster due to the diode across the gate resistor. The drive for each transformer primary is provided by a Microchip TC1404, which is a dual high-speed CMOS driver IC. The dead-time for each MOSFET half-limb is inserted by the dsPIC DSC PWM peripheral module and is selected to avoid any possible shoot-through condition based on the timing delays inherent in the transformer gate drive circuitry.

2.2.1.2 TRANSFORMER

The following section describes a basic procedure for designing the ZVT Full-Bridge transformer. The optimum choice of ferrite core and winding turns/construction is dependent on many factors in the overall converter and may well involve a number of design optimization iterations.

The transformer turns ratio must be selected to ensure that voltage regulation is maintained at the maximum duty limit. As a starting point, D_{max} is assumed to be 0.85, so for the minimum DC link voltage (390V) and the output voltage (12.5V), which includes the voltage drop across the synchronous rectifiers and output chokes, the required transformer turns ratio is 13.3 or less (see Equation 2-12).

An ungapped ETD29 ferrite core pair is selected for the transformer. Table 2-1 lists the various parameters for ETD29 cores made of N87 material.

TABLE 2-1: TRANSFORMER CORE DATA

	A_L (nH/Turn^2)	A_e (mm^2)	V_e (mm^3)	w (mm)	h (mm)	l_m (mm)	R_{th} (ºC/W)
ETD29	2200	76	5350	19.4	4.85	52.8	28

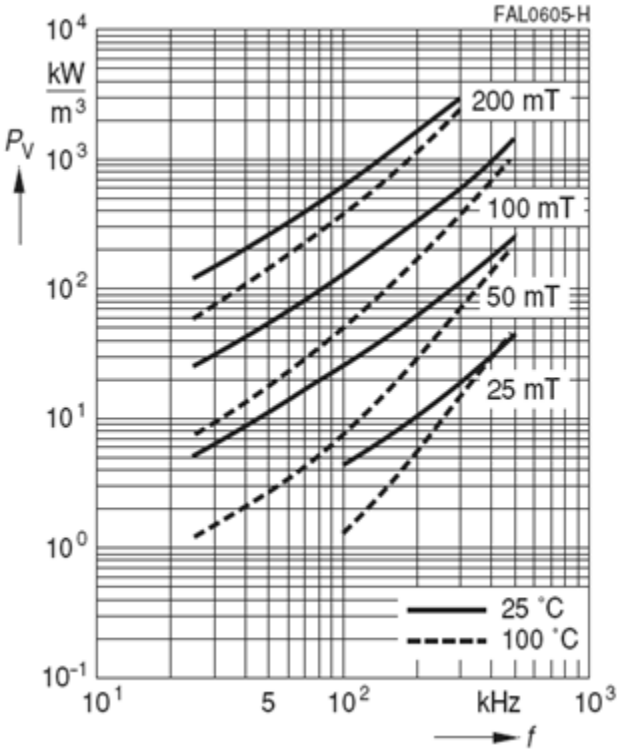
To compute the operating flux density and decide on the number of turns, it is assumed that the maximum allowable transformer temperature rise is 80ºC. The power converter will have forced air cooling from a lid mounted fan so the actual thermal resistance will be about a third less at around 10ºC/W. This means that the total power dissipation can be as much as 8W, with the losses split equally in the copper windings and the ferrite cores. From the core loss curves shown in Figure 2-7, the operating AC peak-to-peak flux density can be as high as 150 mT. The minimum number of turns at the given maximum operating duty is given by Equation 2-14.

EQUATION 2-14:

$$N_{\min} = \frac{V_{in} D_{\max} T}{2 A_e B_{\max}}$$

Therefore, N_{min} is 58, which means that the secondary winding must have either four or five turns to give the required turns ratio computed above. Based on this, a good solution is 64 turns on the primary and five turns on the secondary with a turns ratio, n, of 12.8.

FIGURE 2-7: N87 POWER LOSS CURVES



With the selected turns ratio from Equation 2-12, the actual operating duty, D, is 0.82. Therefore, the operating peak-to-peak flux density is 130 mT at 250 kHz. The core loss in a N87 core can be computed by Equation 2-15.

EQUATION 2-15:

$$P_{core} = 1.36 \times 10^{-4} \, f_{sw}^{1.59} B^{2.74} V_e$$

where f_{sw} is in kHz and B is in mT.

Therefore, the predicted core loss is actually 2.9W. The next stage is now to optimize the winding designs to minimize the losses, especially the high-frequency AC losses due to skin-effect and the proximity effect in multilayer windings (see Reference 5 and Reference 6 in **Appendix C. "References"**). The available winding width, b_w, must be reduced to accommodate a 3 mm creepage border on each side of the bobbin, leaving around 13 mm available for the windings. The total height of the two windings must be less than 4.5 mm which takes into account the layers of 0.05 mm inter-winding tape.

The secondary transformer winding rms current for the current-doubler synchronous rectifier, ignoring inductor ripple current, is given by the relationship shown in Equation 2-16.

EQUATION 2-16:

$$\tilde{I}_{\text{sec}} = \frac{I_o}{2}$$

The secondary rms current is therefore 16.5A, but will be slightly higher in practice due to the magnetizing ramp component of current in the output inductors. For high current windings, copper foil is better suited to utilize the available winding area, and minimize AC copper losses. The secondary winding is a 5 turn strip of copper, and the ideal foil height, h_{id}, in mm is given by Equation 2-17.

EQUATION 2-17:

$$h_{id} = \sqrt{\frac{9.74\times10^3}{N_s f_{sw}}}$$

So h_{id} at 250 kHz is 0.088 mm. The resistance factor, F_R, is given by Equation 2-18.

EQUATION 2-18:

$$F_R = 1+\frac{1}{3}\left(\frac{h}{h_{id}}\right)^4$$

$$\text{when } \frac{h}{h_{id}} < 1.4$$

Therefore, for a practical foil thickness, h, of 0.1 mm, F_R = 1.56. The total resistance including AC effects is given by Equation 2-19.

EQUATION 2-19:

$$r = \frac{F_R l_m}{45\times10^6 b_w h}$$

where l_m is the mean turn length
and b_w is the foil width.

The realistic foil width for the ETD29 is 13.0 mm. This means that the secondary resistance is 1.4 mΩ, which leads to a secondary winding copper loss of about 0.5 W. The current density is actually 14A/mm^2 and, although very high, the power loss is acceptable.

There is no requirement to reduce leakage inductance in the transformer design so the primary winding can be a single winding block. This may also reduce the inter-winding capacitance between primary and secondary and have an impact on EMC. For the low current primary with the large number of turns, round conductors are preferred. Equation 2-20 can be used to identify the ideal wire diameter at the operating frequency, which takes into account skin and proximity effects, and was derived through experimental work by Dowell in the 1960s (see Reference 7 in **Appendix C. "References"**).

EQUATION 2-20:

$$d_{id} = 1.01\left(\frac{17.1 b_w}{SNf_{sw}}\right)^{\frac{1}{3}}$$

where S is the number of strands and N is number of turns in the winding portion.

The resistance factor for round conductors can then be computed from Equation 2-21.

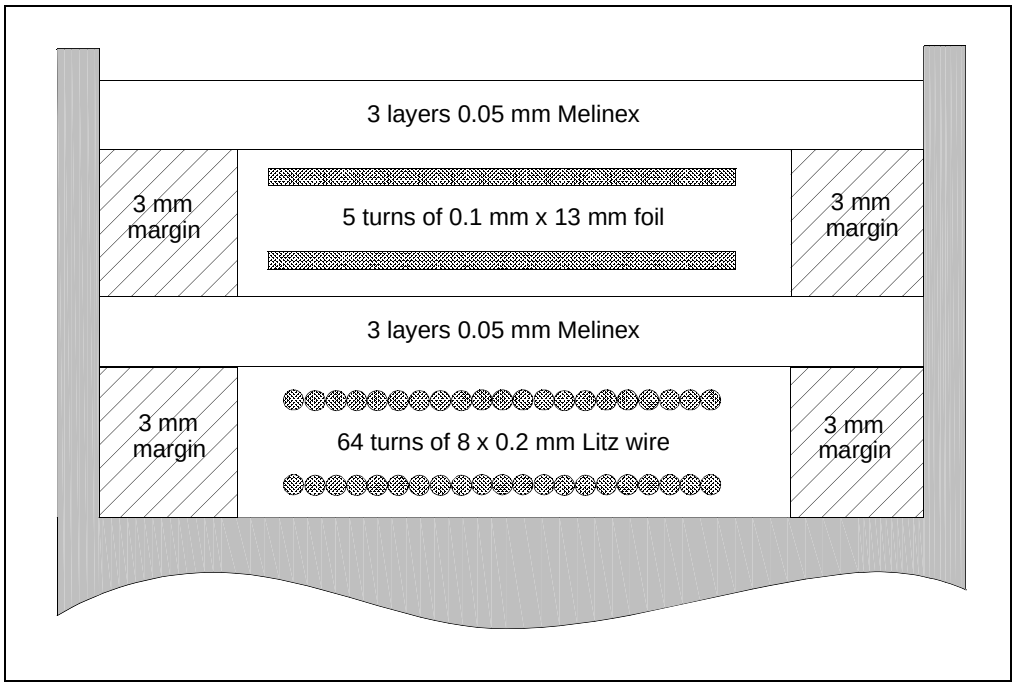
EQUATION 2-21:

$$F_R = 1 + \frac{1}{2}\left(\frac{d}{d_{id}}\right)^6$$

The best fill factor is achieved by using seven-stranded Litz wire, so this is a starting point. Also, assume four layers as an initial starting point with 16 turns per layer. Therefore, the ideal optimum wire diameter is 0.2 mm (32 AWG), giving a resistance factor of 1.5. A commercially available Litz wire has eight strands of 0.2 mm with an OD of 0.75 mm. The DC resistance per meter for single 0.2 mm strand at 100ºC is 0.7074 Ω/m, so the resistance for one mean turn of eight strands is 4.7 mΩ. Therefore, the total adjusted AC resistance of the primary winding is 0.45Ω. The primary current is 1.3 Arms for the estimated secondary current and selected transformer turns ratio, which leads to a primary winding loss of 0.8W. Therefore, the total transformer losses are estimated to be 4.2W in the ETD29 transformer, and will limit the total temperature rise to less than 80ºC with forced air-cooling.

The primary Litz wire has a total OD of around 0.7 mm, so the four-layer primary winding height is about 3 mm. The secondary five-layer foil winding height, including inter-turn insulation, will be around 0.75 mm height, and this design will easily fit in the available 4.85 mm maximum winding window height. The final winding construction is shown in Figure 2-8. The primary winding start and finish are terminated to bobbin pins, while the secondary winding has flying leads which are soldered directly into the PCB.

FIGURE 2-8: ZVT FULL-BRIDGE TRANSFORMER WINDING CONSTRUCTION



The last check is to assess whether an additional inductor is needed for ZVT operation. The leakage inductance (see Reference 8 in **Appendix C. "References"**) for a standard construction transformer is given by Equation 2-22.

EQUATION 2-22:

$$L_L = \frac{4\pi \times 10^{-4} l_m N_p^2}{b_w}\left(c + \frac{h_p + h_s}{3}\right) \quad \mu H$$

where c is the space between the primary and secondary.
All dimensions are in mm.

The ideal computed leakage inductance is 32 µH, which meets the criteria of Equation 2-9 with the MOSFET output capacitance without requiring an additional resonant inductor. Provision has been made on the reference design PCB for an external inductor and parallel capacitors across the MOSFETs if the ZVT operation needs tuning.

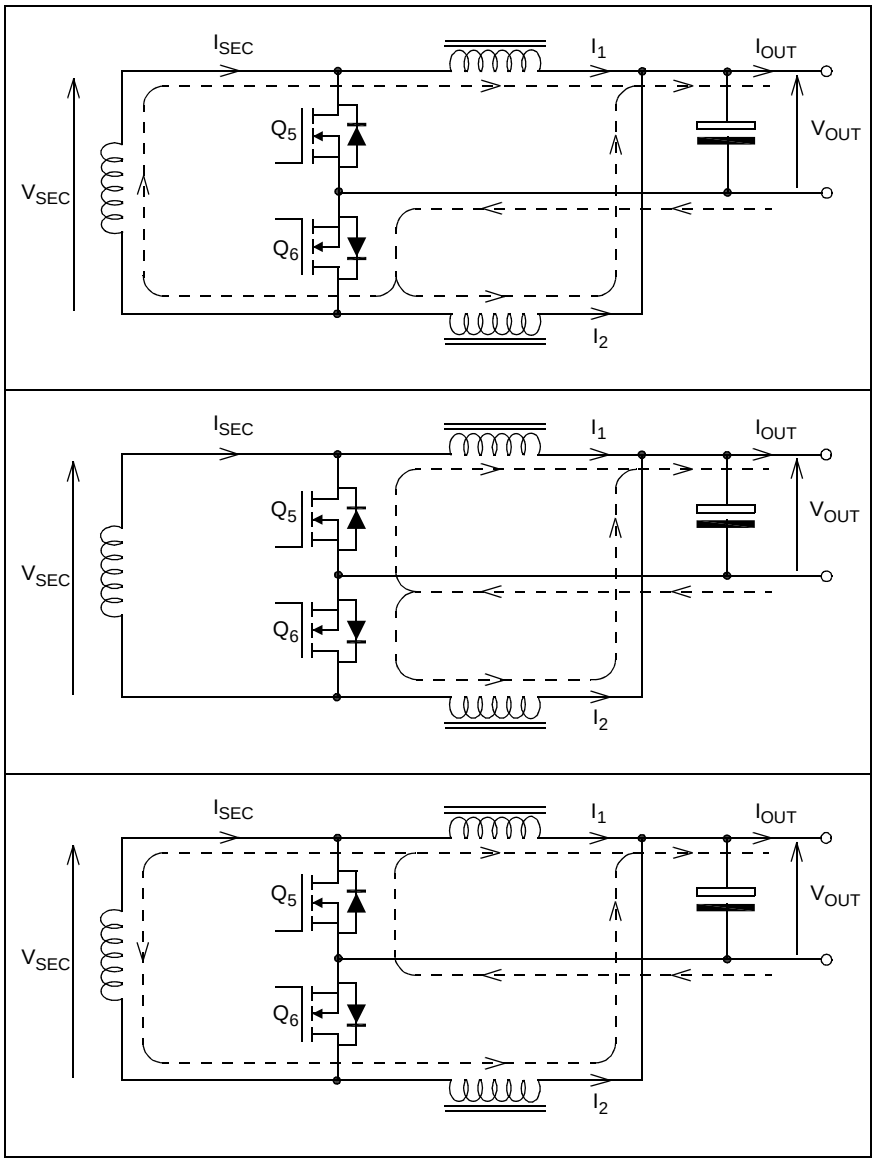
2.2.2 Synchronous Rectifier Design

Synchronous rectification is the technique used for reducing the power loss in the output stage of switched mode power supplies (see Reference 9 in **Appendix C. "References"**). The conventional diode is replaced by a MOSFET and is controlled so that current will flow into the third quadrant in the source-to-drain direction when the equivalent $R_{DS(ON)}$ voltage drop is lower than the intrinsic diode voltage drop. This means that with very low $R_{DS(ON)}$ MOSFETs, the power supply efficiency can be significantly increased. This is especially true in low output voltage power supplies.

In push-pull type power converters, there are a number of synchronous rectifier topologies. In this particular reference design, a current-doubler form has been used (see Reference 10 in **Appendix C. "References"**). Figure 2-9 illustrates the current paths for the four operating modes of the rectifier. The MOSFET commutation is synchronized to the ZVT Full-Bridge switching and gate control signals are generated by the primary-side dsPIC DSC device and fed to the secondary-side via high-speed opto-isolators.

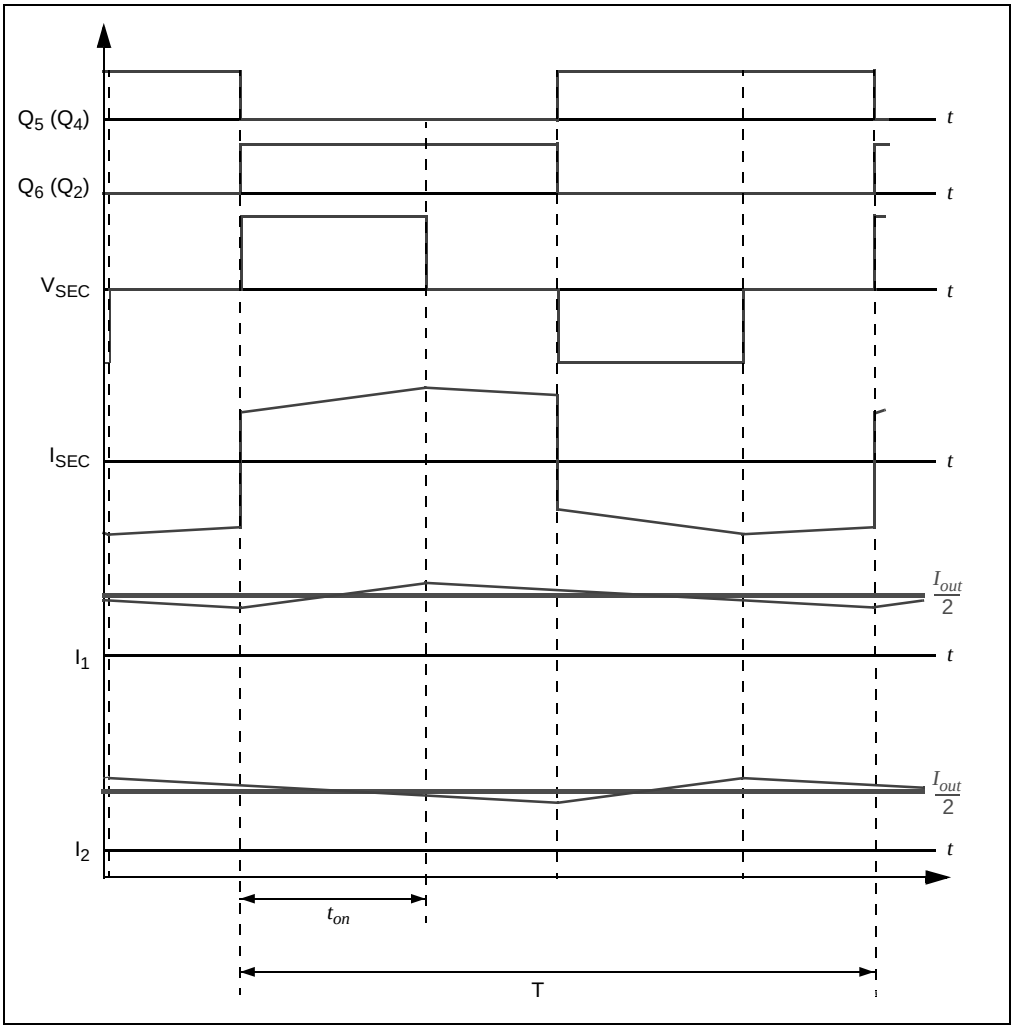
The operating waveforms for the synchronous rectifier are shown in Figure 2-10. As shown in the figure, switch Q6 is gated when the primary current is positive, which coincides with the gating of switch Q2, and Q5 is synchronized with the primary bridge MOSFET Q4 gate signal.

FIGURE 2-9: CURRENT-DOUBLER SYNCHRONOUS RECTIFIER OPERATING MODES



Note: Dotted lines with arrows indicate current polarity.

FIGURE 2-10: SYNCHRONOUS RECTIFIER WAVEFORMS



2.2.2.1 MOSFET SYNCHRONOUS RECTIFIERS AND GATE DRIVES

The MOSFET rectifiers selected for the synchronous rectifier are International Rectifier IRF2804SPBF 40V, 2 mΩ devices. They are packaged in a D^2PAK and mounted directly onto the PCB. The minimum blocking voltage required is equal to the peak applied transformer secondary voltage. With the turns ratio of 12:8 and at the maximum input voltage of 410V, this is 32V. There will be very little overshoot voltage due to the compact layout achieved through mounting on the PCB, and the RC snubber across the secondary winding. The junction to ambient thermal resistance is 40ºC/W when mounted on a 25.4 mm^2 (1 $inch^2$) PCB copper pad (see Reference 11 in **Appendix C. "References"**).

The MOSFET's internal diode voltage characteristic is 0.6V at 30A, 175ºC, which is significantly above the voltage drop across the 2 mΩ ON state resistance, and the benefits of synchronous rectification are maintained over the whole operating power region.

The gate-drive circuit employs a Microchip MCP1403 gate driver. The gate control signals are generated by the primary-side dsPIC DSC device so that they are synchronized with the ZVT Full-Bridge commutation. Isolation is achieved by high-speed opto-isolators.

2.2.2.2 OUTPUT CHOKE

There are two output chokes in the current-doubler synchronous rectifier. Each inductor's mean current is half the output current, and the fluxing voltage period occurs in only half of the cycle. Therefore the ripple current is given by Equation 2-23.

EQUATION 2-23:

$$I_{ripple} = \frac{DT}{2L}\left(\frac{V_{in}}{n} - V_o\right)$$

The choke is designed to have a 20% current ripple component, and the inductance is selected to give 3.3A at the nominal input voltage 400V. Therefore, the inductance needs to be 9 μH and the winding rated for a current of around 18A.

The Magnetics Kool Mu core iron loss can be computed from Equation 2-24.

EQUATION 2-24:

$$P_c = \left(\frac{DT}{2NA_e}\left(\frac{V_{in}}{n} - V_o\right)\right)^2 f_{sw}^{1.46} \qquad \text{W/m}^3$$

The peak flux density is computed from Equation 2-25.

EQUATION 2-25:

$$B_{pk} = \frac{LI_{pk}}{NA_e} \qquad \text{T}$$

Taking the 20.3 mm OD core No. 77848 with an A_L = 32 with A_e = 22.6 mm^2, the required number of turns, N, is 17. Therefore, the peak-to-peak AC flux density is 77 mT and the core loss is 0.5W. According to the single-layer winding data, 1.6 mm OD wire (14 AWG) will fit on the core so that the 13 x 0.315 mm will fit. The copper cross-sectional area is 1.01 mm^2, so the current density is 17.7A/mm^2. The resistance is estimated to be 7 mΩ (double the 14 AWG resistance) and so the copper loss is 2.2W. With forced air-cooling this is acceptable.

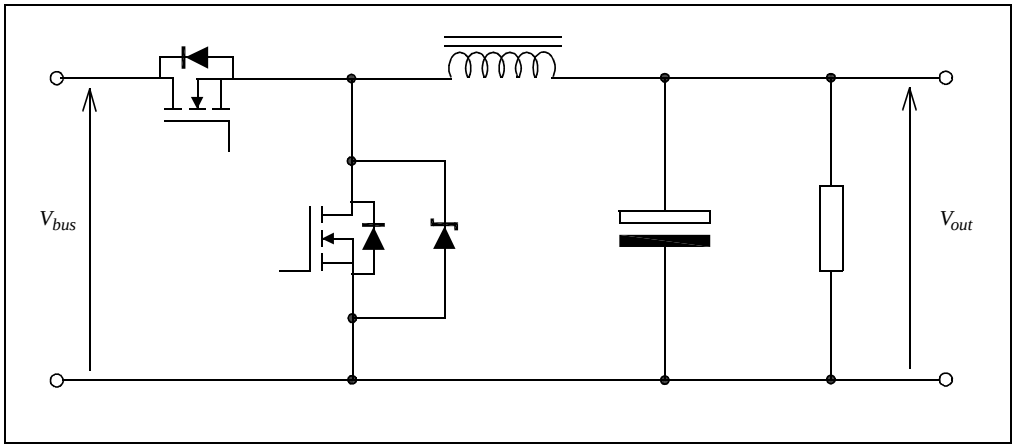
2.2.2.3 OUTPUT CAPACITOR

The main output capacitor is a 2200 μF, 25V electrolytic with two 10 μF, 25V multilayer ceramic capacitors in parallel. The larger bulk capacitance provides the main energy storage while the small ceramic capacitors with very low ESR provide the high-frequency ripple current decoupling capability. The capacitor ripple current is the combined AC components of the two output inductors plus the AC component of the synchronous Buck loads. In the case of the inductor currents, this is lower compared to a conventional output rectifier due to the 50% phase shift in the inductor currents, and is dominated by current supplied to the synchronous Buck regulators. The capacitor must also provide enough energy during a step load transient to maintain the 12V output voltage within the required regulated limits.

2.3 SINGLE-PHASE SYNCHRONOUS BUCK CONVERTER

The Single-Phase Synchronous Buck converter uses the same basic topology as the standard step-down Buck converter, but replaces the free-wheel diode with a MOSFET. Figure 2-11 shows the main power circuitry. The two switches are operated as a complementary pair with a dead-time inserted by the PWM controller to avoid shoot-through. The low-side MOSFET is operated in the third quadrant with current flowing from source to drain when the current is required to free-wheel, and, due to the very lower ON state resistance of the MOSFET, higher efficiency is achieved compared with a conventional Schottky diode.

FIGURE 2-11: SINGLE-PHASE SYNCHRONOUS BUCK CONVERTER



2.3.1 Single-Phase Buck Converter Power-Train Design

The target specification for the Single-Phase Buck converter is as follows:

- Input voltage, VIN = 12 VDC
- Switching frequency, f_{sw} = 500 kHz
- Output voltage, VOUT = 5 VDC
- Output current, IOUT = 23A
- Voltage ripple < 2%
- Output slew rate > 5 A/µs

2.3.1.1 MOSFETS AND GATE DRIVE

The equation governing the duty cycle of a Buck converter is shown in Equation 2-26.

EQUATION 2-26:

$$D = \frac{V_o}{V_{bus}}$$

The rms currents in the high-side and low-side MOSFETs, assuming a low inductor ripple current is as follows in Equation 2-27 and Equation 2-28.

EQUATION 2-27:

$$\tilde{i}_{high} = I_o\sqrt{D}$$

EQUATION 2-28:

$$\tilde{i}_{low} = I_o\sqrt{1-D}$$

The nominal duty cycle is 0.42 ignoring stray voltage drops and inductor current ripple. This equates to a high-side MOSFET on-time, t_{on}, of 840 ns. Therefore, the high-side MOSFET is rated for 14.9 Arms and the low-side MOSFET is rated for 17.5A.

The selected MOSFETs are International Rectifier IRLR7833PBF, 30V, 4.5 mΩ devices in a DPAK package, and are mounted directly on the PCB. The intrinsic reverse diode of the MOSFET is relatively slow in switching, so a fast Schottky diode is placed in parallel across the MOSFET to reduce switching loss. The conduction losses of the high-side and low-side MOSFETs are estimated at 0.85W and 1.2W respectively. It is possible in some designs to optimize the efficiency performance by selecting different devices for the high-side and low-side switches.

The switching loss in the MOSFETs can be estimated by assuming ideal linear switching transitions using Equation 2-29.

EQUATION 2-29:

$$P_{sw} = \tfrac{1}{6}V_{bus}I_o t_r f_{sw}$$

The estimated switching transition time is 50 ns, so the switching loss for each device is 2.4W.

The gate drive circuitry is a dual Microchip MCP1404 gate-drive IC, which drives the MOSFET gates directly. The maximum gate threshold of each MOSFET is 4V, so the drive circuit for the high-side MOSFET is provided by the auxiliary SMPS power rail, which is higher than the gate threshold and source voltage combined. The PWM module pin of the dsPIC DSC device interfaces with the gate-drive IC via an inverting open-collector transistor stage, which provides immunity against ground bounce.

2.3.1.2 OUTPUT CHOKES

The ripple current is given by the relationship shown in Equation 2-30.

EQUATION 2-30:

$$\Delta i = \frac{t_{on}\left(V_{bus} - V_0\right)}{L}$$

The ripple current needs to be less than 25% of the output current so each output choke is a 1 μH Coilcraft SER1360-102KL surface mount. A smaller inductor would improve the output transient response, but at the expense of higher ripple current and, consequently, higher output voltage ripple. The DC resistance is 2.5 mΩ and the power loss is 1.3W for the maximum 23A output current. The peak-to-peak ripple current is 5.9A.

2.3.1.3 OUTPUT CAPACITOR

The output capacitor ripple current is fairly low in a Buck converter due to the continuous inductor current, and is only dependent on the amplitude of ripple current in the inductor. The relationship for capacitor rms current is given by Equation 2-31.

EQUATION 2-31:

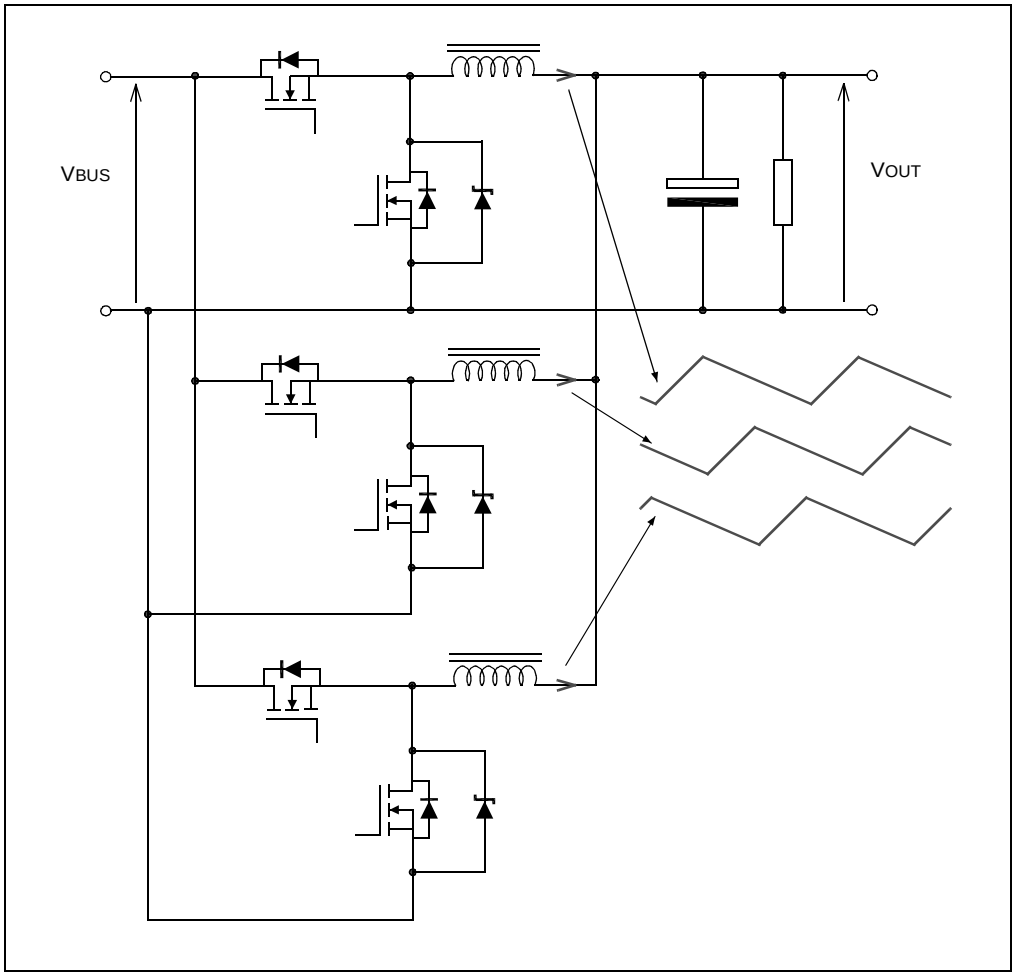
$$\tilde{i}_{cap} = \frac{\Delta i}{\sqrt{12}}$$

Therefore, the total capacitor ripple current is 1.7 Arms. Another important design consideration for the bulk capacitors is the transient load requirements, so low ESR/ESL parts are required to meet the specification (see Reference 12 in **Appendix C. "References"**). Two Rubycon 10ZL1500M10X23 1500 μF, 10V electrolytic capacitors, plus four 10 μF, 16V multi-layer ceramics in parallel were selected. The electrolytic capacitors are each rated to 2.15 Arms at 105ºC, which can easily handle the ripple current on their own.

2.4 THREE-PHASE SYNCHRONOUS BUCK CONVERTER

Multiple synchronous Buck converters can be connected in parallel to increase the power handling of a step-down voltage stage. Performance improvements and a reduction in output capacitor size can be achieved by phase-shifting the PWM modulation in each stage. In this reference design, a Three-Phase Synchronous Buck converter has been designed. The power circuit is shown in Figure 2-12 and illustrates the switching cycle 120 degree PWM phase-shifting in the output choke currents.

FIGURE 2-12: THREE-PHASE SYNCHRONOUS BUCK CONVERTER



2.4.1 Multi-Phase Buck Converter Power-Train Design

The target specification for the Multi-Phase Buck converter is as follows:

- Input voltage, V_{IN} = 12 V_{DC}
- Switching frequency, f_{sw} = 500 kHz
- Output voltage, V_{OUT} = 3.3 V_{DC}
- Output power, I_{OUT} = 69 A
- Voltage ripple < 2%
- Output slew rate > 50A/μs

2.4.1.1 MOSFETS AND GATE DRIVE

The output current for each phase Buck stage is 23A and nominal duty cycle is 0.275 ignoring stray voltage drops and inductor current ripple. This equates to a high-side MOSFET on-time, t_{on}, of 550 ns. Therefore, the high-side MOSFET is rated for 12 Arms, and the low-side MOSFET is rated for 19.6A.

The selected MOSFETs are International Rectifier IRLR7833PBF, 30 V, 4.5 mΩ devices in a DPAK package, and are mounted directly on the PCB. The conduction losses of the high and low-side MOSFETs are estimated at 0.55W and 1.5W respectively. The estimated switching transition time is 50 ns, so the switching loss for each device is 1.2W.

The gate drive circuitry is a dual Microchip MCP1404 gate-drive IC, which drives the MOSFET gates directly. The maximum gate threshold of each MOSFET is 4V, so the drive circuit for the high-side MOSFET is provided by the auxiliary SMPS power rail, which is higher than the gate threshold and source voltage combined. The PWM module pin of the dsPIC DSC device interfaces with the gate-drive IC via an inverting open-collector transistor stage which provides immunity against ground bounce.

EQUATION 2-32:

$$D = \frac{V_o}{V_{bus}}$$

$$i_{high} = I_o\sqrt{D}$$

$$i_{low} = I_o\sqrt{1-D}$$

$$P_{sw} = \tfrac{1}{6} V_{bus} I_o t_r f_{sw}$$

2.4.1.2 OUTPUT CHOKES

The ripple current in each inductor is given by the relationship shown in Equation 2-33.

EQUATION 2-33:

$$\Delta i = \frac{t_{on}\left(V_{bus} - V_0\right)}{L}$$

The ripple current needs to be about 20% of the output current; therefore, each output choke is a 1 μH Coilcraft SER1360-102KL surface mount. The DC resistance is 2.5 mΩ and the power loss is 1.3W. The peak-to-peak ripple current is 4.8A.

2.4.1.3 OUTPUT CAPACITOR

The output capacitor ripple current is very low due to the continuous inductor currents with phase shifting. The relationship for capacitor rms current is given by Equation 2-34.

EQUATION 2-34:

$$\tilde{i}_{cap} = \frac{\Delta i}{\sqrt{3}\sqrt{12}}$$

Therefore, the total capacitor ripple current is 1.0 Arms. The output capacitor is made up of three Rubycon 6.3ZL1500M10X20 1500 μF, 6.3V electrolytic capacitors plus three 10 μF, 16V multi-layer ceramics in parallel. The electrolytic capacitors are each rated to 1.82 Arms at 105ºC, and can easily handle the ripple current on their own.

2.5 AUXILIARY POWER SUPPLY

The supply voltages for the primary and secondary side dsPIC DSC device and gate drive circuitry are generated by a simple low-power flyback SMPS. Figure 2-13 illustrates the main components in the design. The integrated high-voltage proprietary controlled switch feeds a high-frequency transformer, and multiple secondary windings tapped-off via a diode/capacitor circuit. The SMPS operates in discontinuous flyback mode, so that energy is stored in the magnetizing inductance of the transformer during the switch on-period, and transferred to the secondary circuits during the off-period. A snubber arrangement is required across the transformer primary to dissipate the transformer parasitic leakage energy and ensure that the switch voltage does not exceed its maximum rating. The typical flyback MOSFET waveforms are shown in Figure 2-14.

FIGURE 2-13: AUXILIARY FLYBACK SMPS

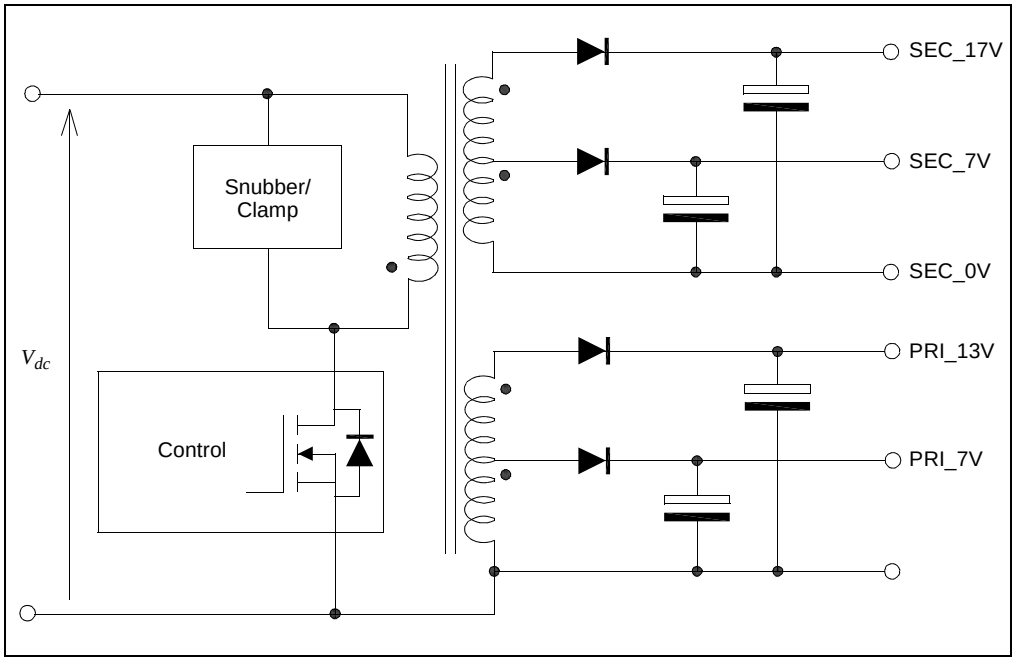
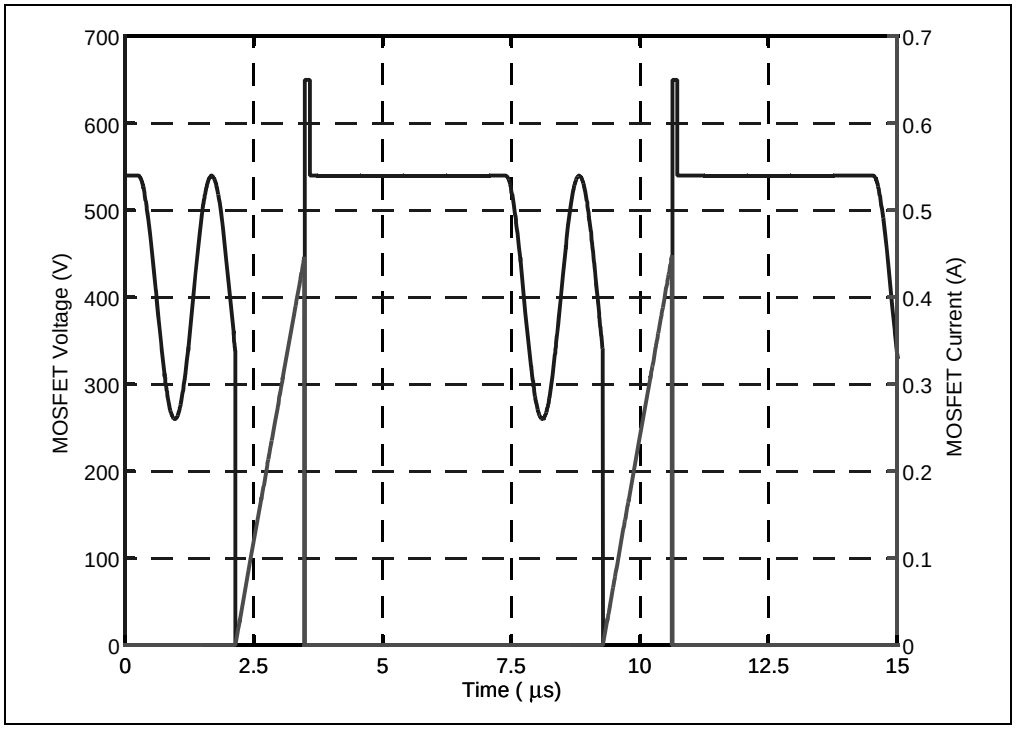


FIGURE 2-14: FLYBACK SMPS MOSFET WAVEFORMS



2.5.1 Basic Design Methodology

The target specification for the auxiliary flyback SMPS is as follows:

- Input voltage, V_{IN} = 120-400 V_{DC}
- Primary Output Rail 1 = 7V @ 0.3A
- Primary Output Rail 2 = 13V @ 0.15A
- Secondary Output Rail 1 = 7V @ 0.3A
- Secondary Output Rail 2 = 17V @ 0.45A

2.5.1.1 HVIC TECHNOLOGY

The total output power rating of the auxiliary power supply is 13.8W; therefore, a Power Integrations TinySwitch (see Reference 13 in **Appendix C. "References"**) was selected for the main power switch. These devices are intended specifically for low-cost high-efficiency designs and operate with simple ON/OFF control rather than more sophisticated PWM common to higher power SMPS. The TNY277G is a suitably rated part for this wide input voltage application, and can be mounted directly on the PCB without any additional cooling requirements.

2.5.1.2 TRANSFORMER

Based on the operating frequency and power throughput requirement, an EF20 ferrite core pair is selected for the transformer design. The first step in the design is to select the number of primary turns and transformer air-gap. Discontinuous flyback SMPS output power is dictated by the energy stored in the primary magnetizing inductance of the transformer and the switching frequency. The basic equation, ignoring losses, is shown in Equation 2-35.

EQUATION 2-35:

$$P_o = \tfrac{1}{2} L_p I_p^2 f_{sw}$$

The peak current in the primary is fixed for a given output power and the switch on-time varies as a function of the DC input voltage, as shown in Equation 2-36.

EQUATION 2-36:

$$t_{on} = \frac{L_p I_p}{V_{DC}}$$

From the TNY277 data sheet, the maximum switching frequency is 140 kHz, and a sensible maximum on-time is 4.5 μs. The minimum DC voltage is 120V, and the power at the transformer primary is 17W, assuming ~ 80% efficiency. It is worth noting that this is only a transient requirement, since once the dsPIC DSC device rails are established, the PFC will boost the DC input voltage to 400V. Equation 2-35 and Equation 2-36 can be rearranged to find the required primary magnetizing inductance of the transformer, as shown in Equation 2-37.

EQUATION 2-37:

$$L_p = \frac{t_{on}^2 V_{DC}^2 f_{sw}}{2 P_o}$$

Therefore, the target primary inductance is 1.2 mH and the peak primary current is 0.45A. The primary turns must be selected to ensure that the ferrite core losses are around 0.5W for thermal reasons. The EF20 core has a cross-sectional area of 32 mm^2 and a volume of 1490 mm^3.

The core loss can be computed from Equation 2-38.

EQUATION 2-38:

$$B = \left(\frac{P_{core}}{1.36 \times 10^{-4} f_{sw}^{1.59} V_e} \right)^{0.365}$$

where f_{sw} is in kHz and B is in mT.

Therefore, the peak flux density is about 150 mT. The required number of primary turns can be computed using Equation 2-39.

EQUATION 2-39:

$$B = \frac{L_p I_p}{N_p A_e}$$

Using the above formula, N_p is set at 110 turns, which requires a 0.5 mm air-gap in the EF20 core to give 1.2 mH inductance. To minimize the leakage inductance of the transformer, and hence the loss in the snubber/clamp, the primary winding is split into two layers of 55 turns each. The rms current in the primary is given by Equation 2-40.

EQUATION 2-40:

$$\tilde{i}_p = \sqrt{\frac{D}{3}} I_p$$

From Equation 2-36, the on-time for the switch at 400V is 1.35 μs and the duty cycle is 0.19. Therefore, the rms current in the primary is 0.11 Arms. A suitable winding wire diameter is 0.16 mm with 5.5 Amm^{-2}. The 100ºC resistance of this wire is 1.1 Ωm^{-1}, and from the mean turn length of the bobbin (41.2 mm), the predicted primary resistance is 5Ω. Therefore, the primary copper loss is 60 mW.

The secondary turns must be selected to ensure that the referred voltage across the TNY277 does not exceed its maximum blocking voltage rating and for discontinuous current operation given the operating duty cycle. The peak voltage across the TNY277 when energy is transferred to the secondary is given by Equation 2-41.

EQUATION 2-41:

$$V_p = V_{DC} + \frac{N_p}{N_s} V_o$$

A sensible limit on the maximum switch voltage is 540V, so for the main 17V secondary output, including a 0.8V diode forward voltage drop, the required turns ratio is 7.86. Therefore, the secondary turns on the 17V winding is 14. A separate tapping at six turns on this winding can be used for the 7V secondary. The secondary winding is constructed using TEX-E wire to give the required 2500 Vrms galvanic voltage isolation.

The time taken for the flyback transformer to be de-fluxed is given by Equation 2-42.

EQUATION 2-42:

$$t_{off} = \frac{N_s L_p I_p}{N_p V_o}$$

Therefore, the off period is 3.9 μs, which is lower than the maximum available period to ensure discontinuous operation under normal operating conditions.

The secondary peak and rms currents in the winding are given by the following formula in Equation 2-43 and Equation 2-44.

EQUATION 2-43:

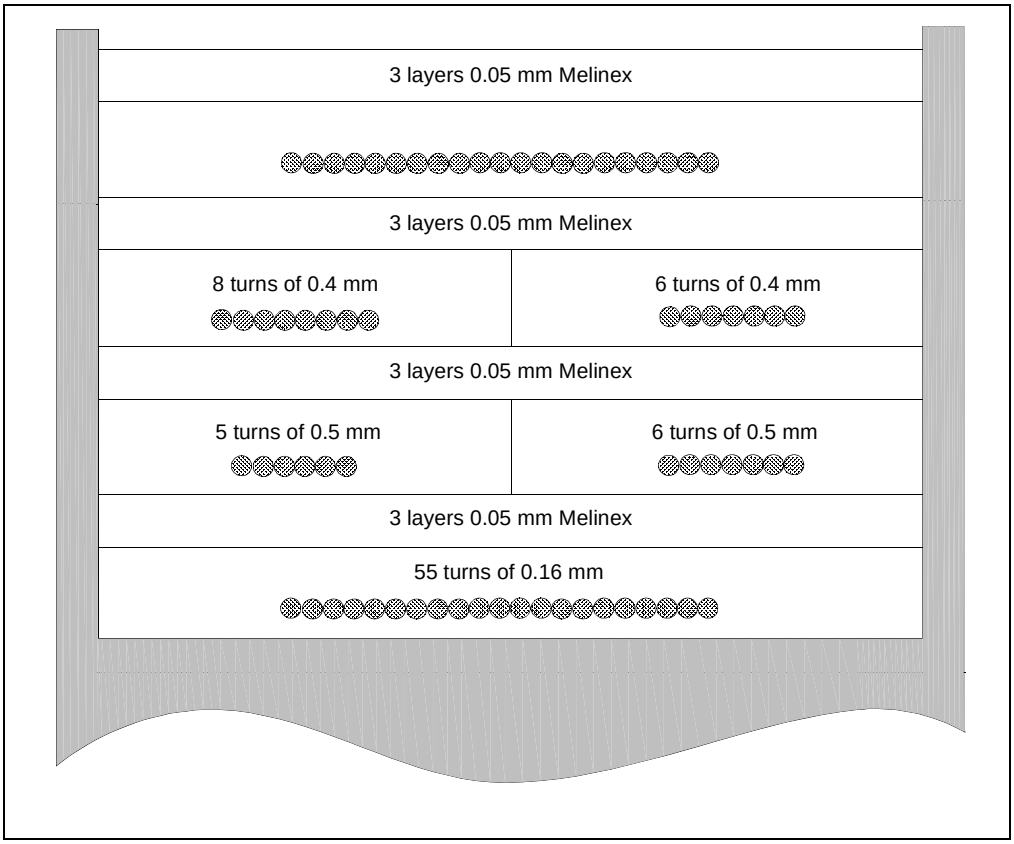
$$I_s = \frac{2TI_o}{t_{off}}$$

EQUATION 2-44:

$$\tilde{i}_s = 2\sqrt{\frac{T}{3t_{off}}} I_o$$

Therefore, the secondary current in the main 17V output is 0.7 Arms. The secondary winding resistance is 0.1Ω and the total copper loss in the secondary winding is estimated to be 50 mW. Keeping a similar winding current density as the primary means that a 0.4 mm wire gauge can be chosen for the secondary windings. The two auxiliary supply windings on the primary side follow directly from the chosen transformer turns ratio. The total transformer power dissipation is dominated by the iron loss and is roughly 0.8W. This will lead to a temperature rise of 40ºC, based on the published thermal characteristics of an EF20 transformer. Figure 2-15 illustrates the flyback transformer construction.

FIGURE 2-15: FLYBACK TRANSFORMER CONSTRUCTION



2.5.1.3 OUTPUT CAPACITORS

The capacitors selected for outputs are 100 μF, 25V and 470 μF, 10V, for gate drive voltage rails and the dsPIC DSC device voltage rails, respectively. The ripple current rating for United Chemi-Con electrolytic capacitors are 0.34 Arms and 0.64 Arms, respectively.

NOTES:

Chapter 3. Software Design

3.1 OVERVIEW

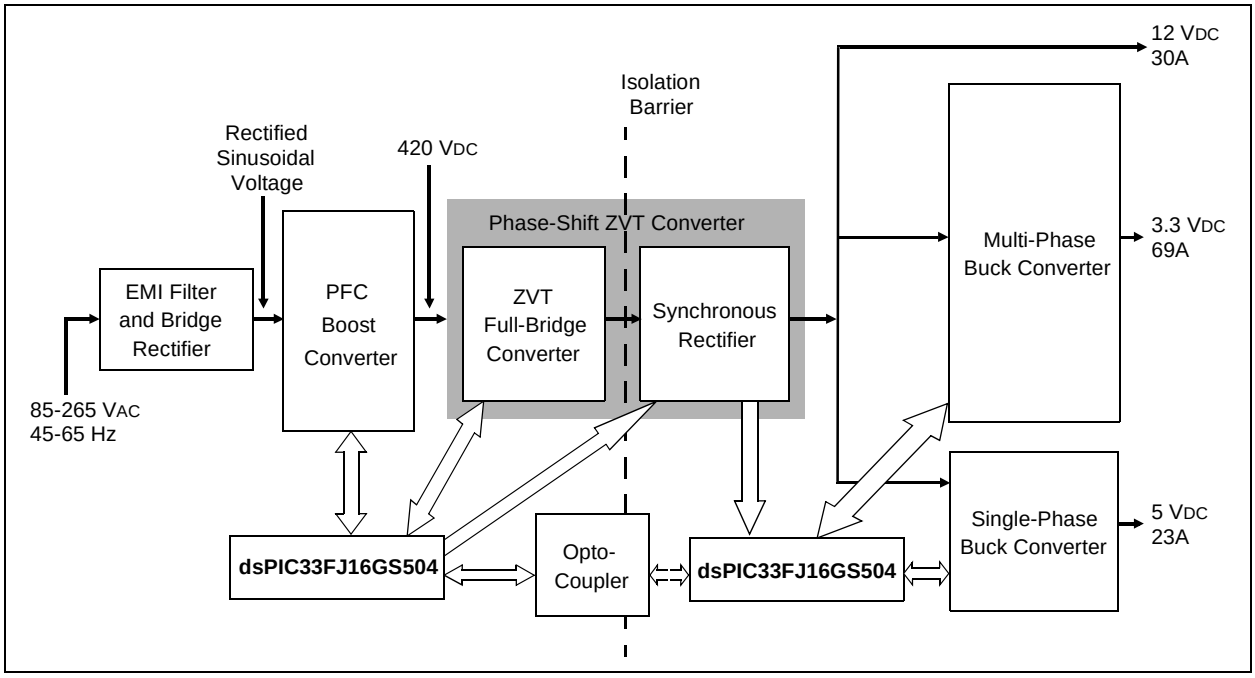
Note: Any libraries and source files associated with SMPS AC/DC Reference Design are available by request from your local Microchip sales office. See the Microchip Web site, or the last page of this document for contact information.

The SMPS AC/DC Reference Design is controlled using two dsPIC DSCs as shown in the block diagram in Figure 3-1.

The dsPIC DSC on the primary side (on the left of the isolation barrier in Figure 3-1) controls the PFC Boost Converter and the Phase-Shift ZVT Converter. The dsPIC DSC on the secondary side (on the right of the isolation barrier in Figure 3-1) controls the Multi-Phase Buck Converter and the Single-Phase Buck Converter.

The secondary side dsPIC DSC also performs the function of measuring the output voltage of the Phase-Shift ZVT Converter, and feeding back to the primary side dsPIC DSC as a digital feedback signal.

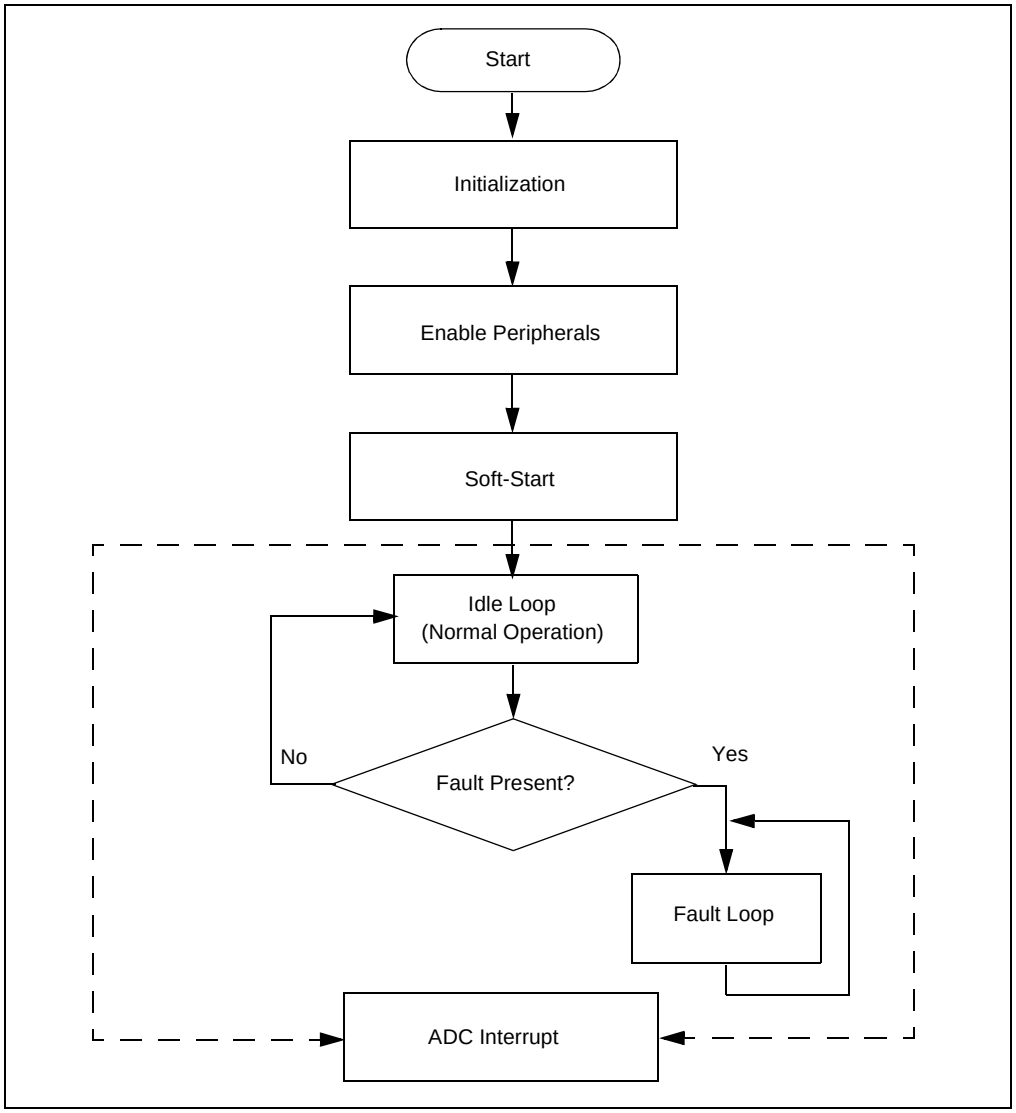
FIGURE 3-1: BLOCK DIAGRAM OF SMPS AC/DC REFERENCE DESIGN



3.2 STRUCTURE OF THE CONTROL SOFTWARE

The control software for the SMPS AC/DC Reference Design essentially follows a single basic structure as shown in Figure 3-2.

FIGURE 3-2: FLOWCHART OF CONTROL SOFTWARE



The control software uses a mixture of C programming and Assembly programming. All time-critical functions are written in Assembly language. The main loop, peripheral setup routines, initialization routines and non-critical functions are all written using the C programming language.

The SMPS AC/DC Reference Design comprises of two separate projects, namely:

- **Primary:** This project contains the complete code for the primary side of the SMPS AC/DC Reference Design. This includes the control software for the PFC Boost Converter and the Phase-Shift ZVT Converter.
- **Secondary:** This project contains the complete code for the secondary side of the SMPS AC/DC Reference Design. This includes the control software for the Single-Phase Buck Converter and Multi-Phase Buck Converter, and also includes code for the ZVT output voltage measurement and digital voltage feedback.

All of the functional blocks shown in Figure 3-2 are common to both projects. Brief descriptions of each functional block are provided in subsequent sections.

3.2.1 Initialization Routine

The initialization routines are called from the main program at the start of execution. All peripherals including PWM, ADC, analog comparator, UART, I^2C™ and Timers are configured in this step. It is important that none of the peripherals are enabled before the entire peripheral configuration is completed.

In addition to configuring the peripherals, all required interrupts and interrupt priorities are configured in the initialization step. Memory allocation for control loop variables is also done during the initialization stage.

3.2.2 Peripheral Enable Routine

After configuring all peripheral modules that are used in the project, we enable them in the correct sequence. Since the PWM output directly affects the output of the system, it is important to enable it after all other peripherals have been enabled.

3.2.3 Soft-Start Routine

Each individual stage of the SMPS AC/DC Reference Design employs a controlled soft-start routine. This routine ramps individual output stages to the desired output voltage.

3.2.4 Fault Check Routine

The fault check routine is used to check for faults that have occurred in the system. If a fault has occurred, the system has to be shut down. To do this, the fault loop is called and used to disable all active modules, such as the ADC and PWM, and to visually display the fault on the LEDs.

The PWM module on the dsPIC33FJ16GS504 has built-in fault inputs that ensure a fast PWM shutdown in order to prevent damage to the system and downstream electronics. After the PWM is shutdown, the program execution jumps to the fault loop.

3.2.5 ADC Interrupt Service Routine

The ADC Interrupt Service Routine (ISR) is the heart of the control software. All control loops are executed in the ISR. Since faster control loop execution is desired for the best system performance, functions executed in this routine are written in Assembly language. The ADC ISR has the highest priority of execution.

The ADC module is configured to generate interleaved interrupt requests in order to execute multiple control loops within the same ISR.

The implementation of the control software for each stage of the SMPS AC/DC Reference Design contains all the blocks described above. However, there are subtle differences in the implementation for each stage.

Specific details for each stage of the design are covered in subsequent sections of this user’s guide.

3.3 PRIMARY SIDE CONTROL SOFTWARE (PFC_ZVT)

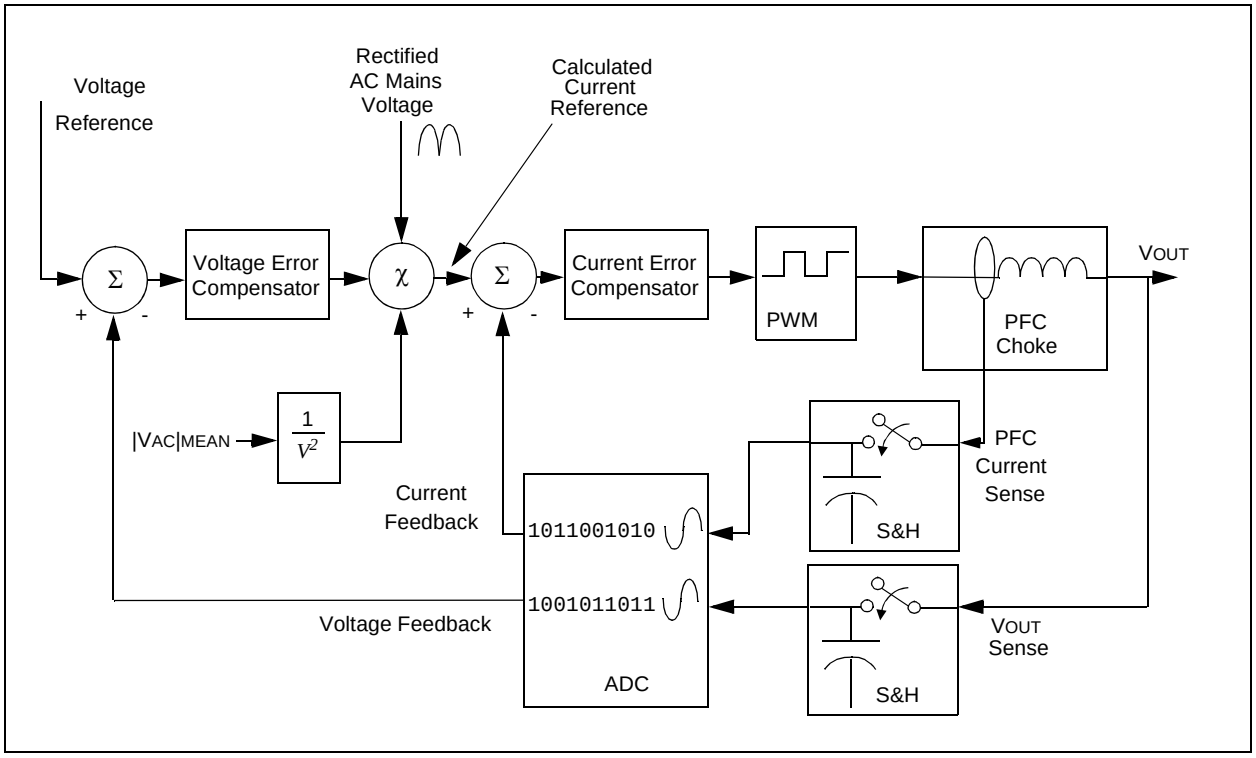
The PFC Boost Converter and Phase-Shift ZVT Converter follow a similar control scheme. However, there are significant differences in the operation of these two converters. These differences will be explained in the description of the control software for each converter.

3.3.1 PFC Boost Converter Control Software

3.3.1.1 PFC CONTROL SCHEME

The control scheme implemented for the PFC Boost Converter is shown in Figure 3-3.

FIGURE 3-3: PFC CONTROL SCHEME



The PFC Boost Converter uses an outer voltage loop and inner current loop control scheme. The output of the voltage error compensator is multiplied by a function of the rectified AC mains voltage to generate a sinusoidal current reference.

An additional feed-forward term is introduced, $|V_{AC}|_{MEAN}$, at the output of the voltage error compensator to make the control loop immune to fluctuations in the AC input voltage. This feed-forward term ensures that the PFC Boost Converter always delivers the correct output power for the entire input voltage range.

The PFC voltage and current error compensators are both implemented as Proportional-Integral (PI) systems with excess error compensation. The compensator functions are math intensive routines and utilize the DSP engine of the dsPIC DSC. The output of the PFC Current compensator modifies the PWM duty cycle to maintain a constant output voltage and also a sinusoidal input current waveform.

Both the current and voltage compensators are executed in the ADC ISR. The current control loop is executed at a much faster rate compared to the voltage control loop.

3.3.1.1.1 Digital PFC Implementation Using the dsPIC DSC

Figure 3-4 shows the hardware resources utilized on the primary side dsPIC DSC for Power Factor Correction.

FIGURE 3-4: dsPIC® DSC RESOURCE ALLOCATION FOR PFC BOOST CONVERTER

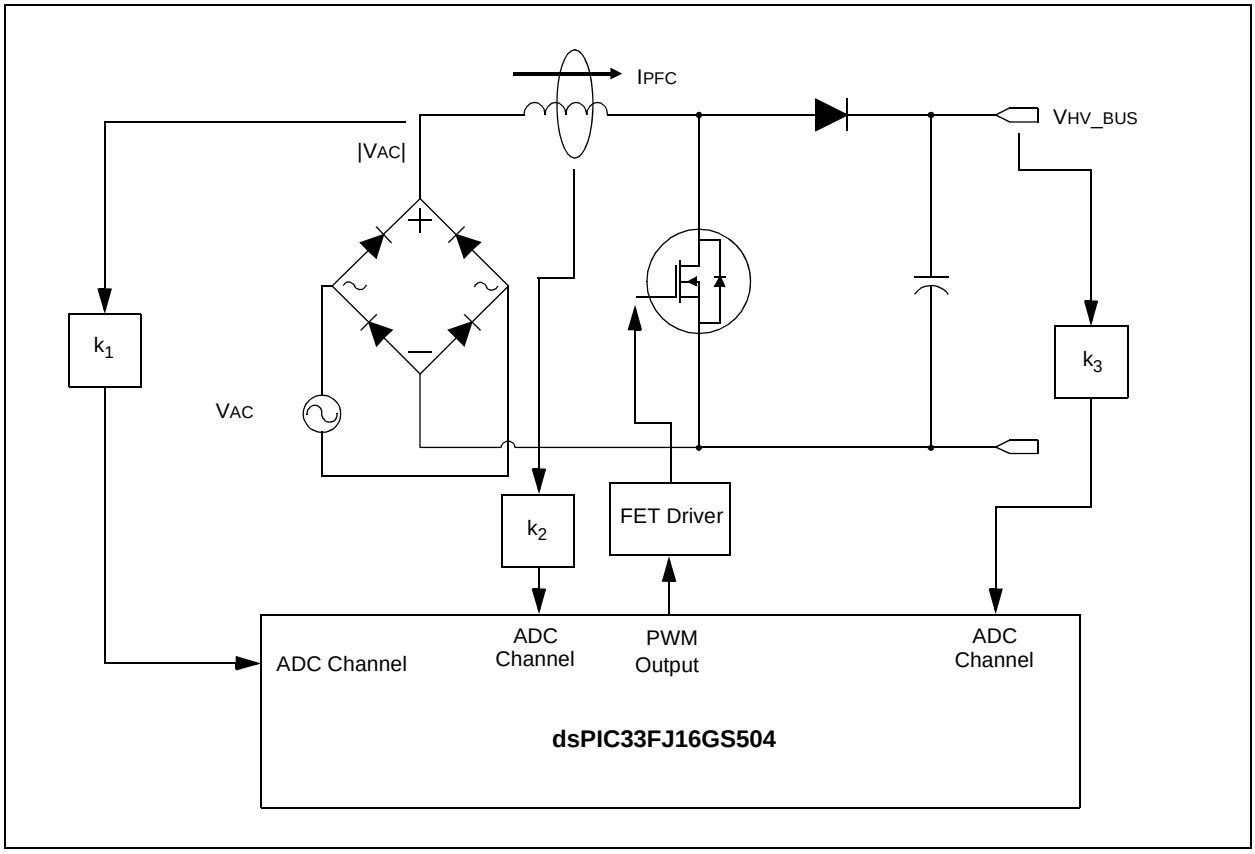


Table 3-1 lists the resources used on the dsPIC DSC for implementing the PFC control scheme shown in Figure 3-3.

TABLE 3-1: dsPIC® DSC RESOURCES FOR PFC BOOST CONVERTER

Description	Type of Signal	dsPIC® DSC Resource Used
VHV_BUS	Analog Input	AN5
PFC Current (IPFC)	Analog Input	AN4
|VAC| Sense	Analog Input	AN3
MOSFET Gate Drive	Drive Output	PWM4L

The control of the PFC Boost Converter is obtained by varying the duty cycle of the PWM signal. Only one pin of the PWM is utilized for the PFC control scheme, and therefore the PWM module is configured for independent output mode. The frequency of the PWM is determined by the hardware design. It is configured to be approximately 125 kHz.

The Analog Inputs AN4 and AN5 are configured to sample simultaneously. A conversion is triggered on both AN4 and AN5 once every 3 PWM cycles, and the current loop is executed on every conversion. The voltage loop is executed only once in 15 current loop executions.

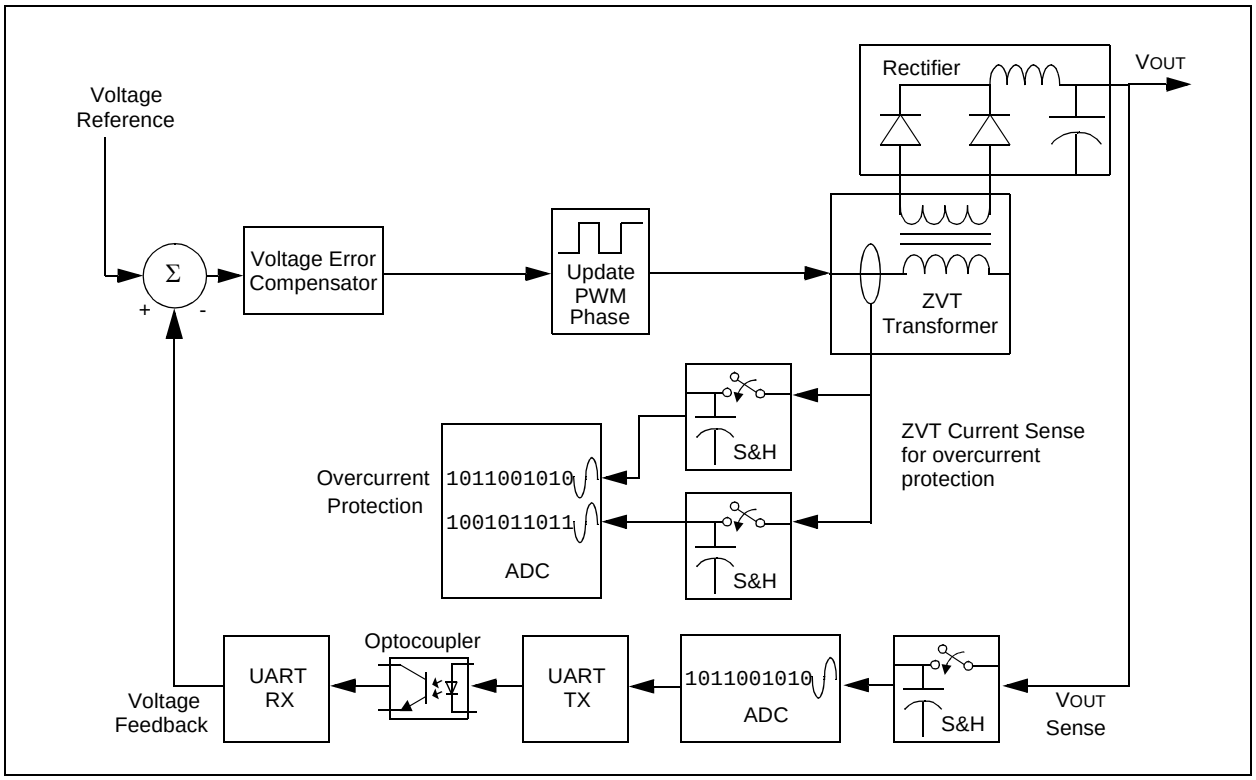
The Analog Input AN3 measures the AC Input voltage, which is used for generating a sinusoidal current reference. In the SMPS AC/DC Reference Design, the current reference value is calculated when the current loop is executed.

3.3.2 Phase-Shift ZVT Control Scheme

3.3.2.1 ZVT RESOURCE ALLOCATION

The control scheme for the Phase-Shift ZVT Converter is shown in Figure 3-5. A schematic of the Phase-Shift ZVT Converter is shown in Figure 3-6.

FIGURE 3-5: PHASE-SHIFT ZVT CONVERTER CONTROL SCHEME



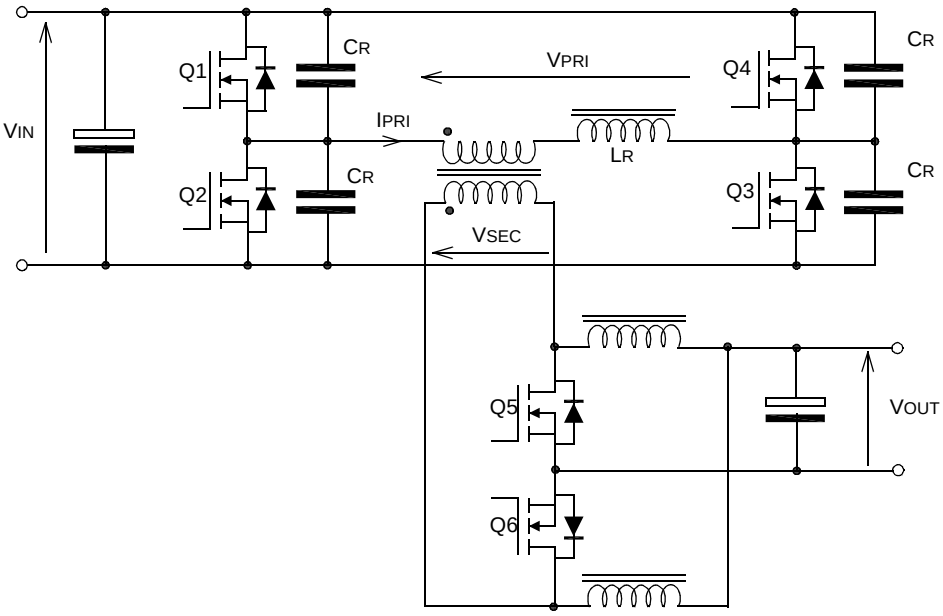
The ZVT converter uses voltage mode control to maintain a constant output voltage. The circuit configuration of the ZVT converter has the output voltage (the parameter to be controlled) on the secondary side of the isolation barrier (refer to Figure 3-8).

The SMPS AC/DC Reference Design implements the ZVT voltage feedback by measuring the output voltage using the secondary side dsPIC DSC. The Most Significant 8 bits of data are transmitted back to the primary side dsPIC DSC through a UART communication channel.

The data received by the primary side dsPIC DSC is right-shifted by two bits (for 10-bit data) and is compared with the voltage reference to produce the voltage error. The voltage error compensator is then executed in the ADC ISR.

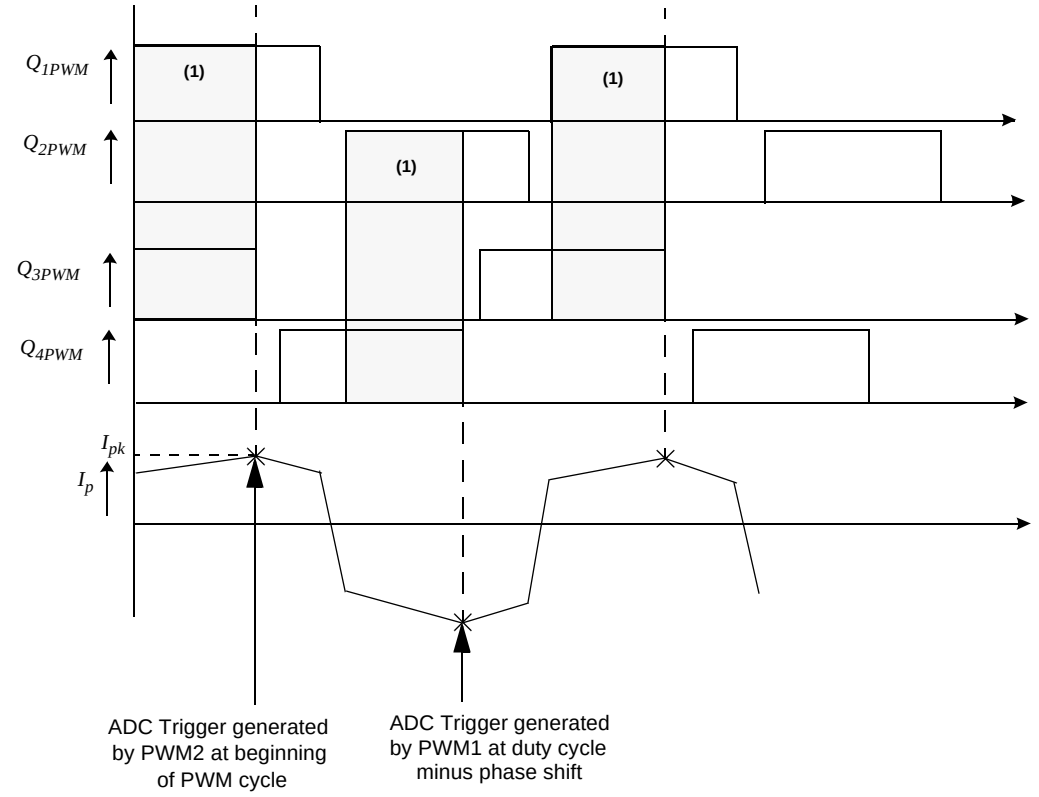
The output of the voltage error compensator is feed into the phase-shifted PWM. The Phase-Shift ZVT converter uses the unique phase-shifting capability of the PWM module in the dsPIC33FJ16GS504. The phase of the PWM signal can be modified by simply writing the new value in the appropriate Special Function Register in the PWM module.

FIGURE 3-6: ZVT PHASE-SHIFT CONVERTER



Current sensing for the Phase-Shift ZVT Converter uses two dedicated analog inputs to measure the primary transformer current in both directions. The two analog inputs are tied to the same current signal, but are sampled at opposite current peaks. The precise triggering instants are in Figure 3-7 along with the expected current waveform. The current in the positive and negative directions must be measured and checked for any imbalance. If the currents in the two directions are not balanced, it may cause a phenomenon called “flux walking” in the ZVT transformer. Flux walking must be prevented since it may lead to transformer saturation and subsequent damage to the system hardware.

FIGURE 3-7: ZVT CURRENT SAMPLING INSTANTS



Note 1: The shaded regions represent the times when power is transferred from the primary side to the secondary side. This region is sometimes referred to as the "effective" ZVT duty cycle.

The voltage compensator is implemented as a Proportional-Integral-Derivative (PID) function. The voltage compensator is executed in the ADC ISR.

3.3.2.2 PHASE-SHIFT ZVT IMPLEMENTATION USING THE dsPIC DSC

FIGURE 3-8: dsPIC® DSC RESOURCE ALLOCATION FOR PHASE-SHIFT ZVT CONVERTER

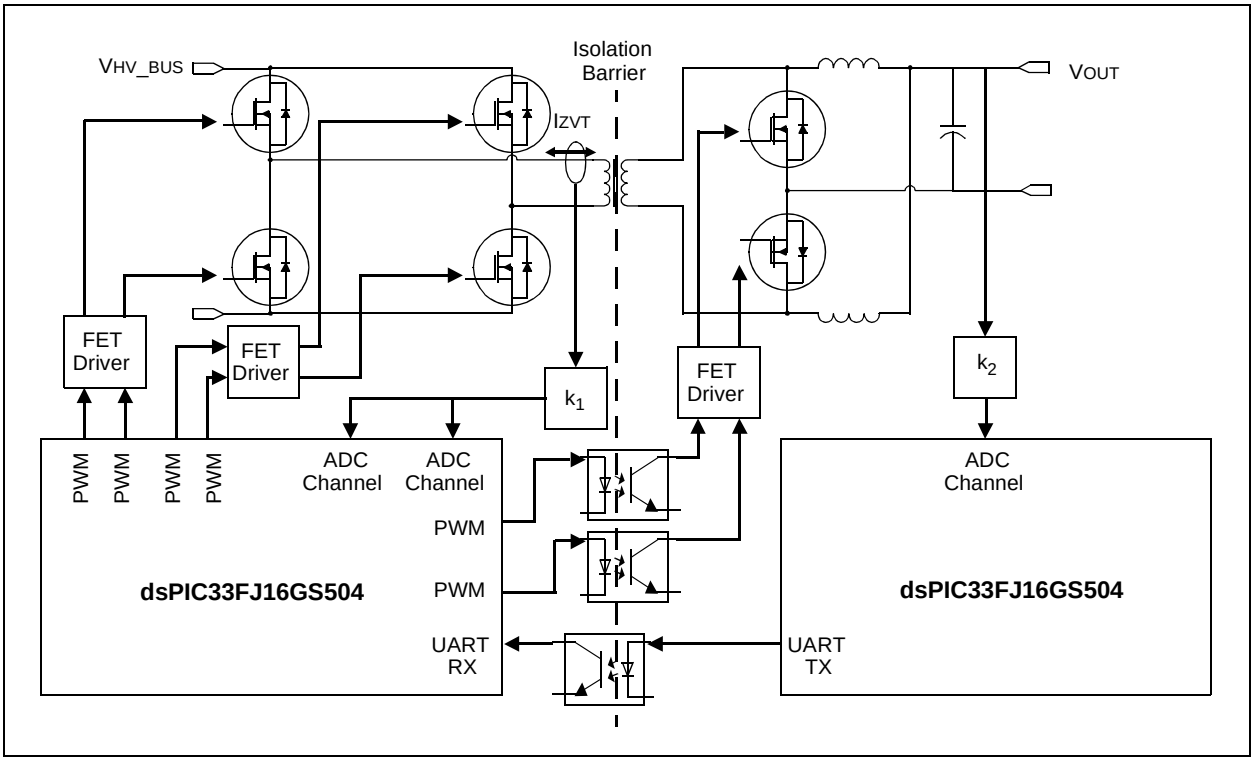


Table 3-2 lists the resources used on the primary side dsPIC DSC for the different feedback and control signals required for the Phase-Shift ZVT Converter control scheme. Table 3-3 lists resources used on the secondary side dsPIC DSC, also required for the Phase-Shift ZVT Converter control scheme.

TABLE 3-2: PRIMARY SIDE dsPIC® DSC RESOURCES FOR PHASE-SHIFT ZVT CONVERTER

Description	Type of Signal	dsPIC® DSC Resource Used
ZVT Current 1 (IZVT1)	Analog Input	AN0
ZVT Current 2 (IZVT2)	Analog Input	AN2
VOUT Feedback	UART Input	U1RX
Full-Bridge Gate Drive	Drive Output	PWM1H, PWM1L, PWM2H, PWM2L
Synchronous Rectifier Gate Drive	Drive Output	PWM3H, PWM3L

TABLE 3-3: SECONDARY SIDE dsPIC® DSC RESOURCES FOR PHASE-SHIFT ZVT CONVERTER

Description	Type of Signal	dsPIC® DSC Resource Used
Voltage Sense (VOUT)	Analog Input	AN5
VOUT Feedback	UART Output	U1TX

The Phase-Shift ZVT Converter is controlled by modifying the phase of the PWM drive signals of one leg of the Full-Bridge relative to the drive signals of the other leg of the Full-Bridge.

As specified in Table 3-2, PWM1H, PWM1L, PWM2H, and PWM2L are the PWM signals used for switching the Full-Bridge MOSFETs. PWM1H and PWM1L control one leg of the Full-Bridge, while PWM2H and PWM2L control the second leg of the Full-Bridge.

PWM1 and PWM2 are configured to operate in the complementary PWM mode and approximately 250 kHz switching frequency. The duty cycle of these PWM signals is fixed at 50%. Some dead time is also inserted to prevent shoot-through.

PWM3 is used for driving the synchronous rectifier MOSFETs on the secondary side of the ZVT Transformer. PWM3 is also configured as a complementary mode PWM signal with dead time. The PWM3 signal is configured identically to that of PWM1. The output of the control loop directly modifies the phase of PWM2 to accomplish the control of the output.

AN0 and AN2 both measure the ZVT current, but each input is sampled on opposite peaks of the current signal. The conversion result of AN0 is used for the ZVT overcurrent fault protection. The voltage feedback is received on the U1RX pin of the primary side dsPIC DSC.

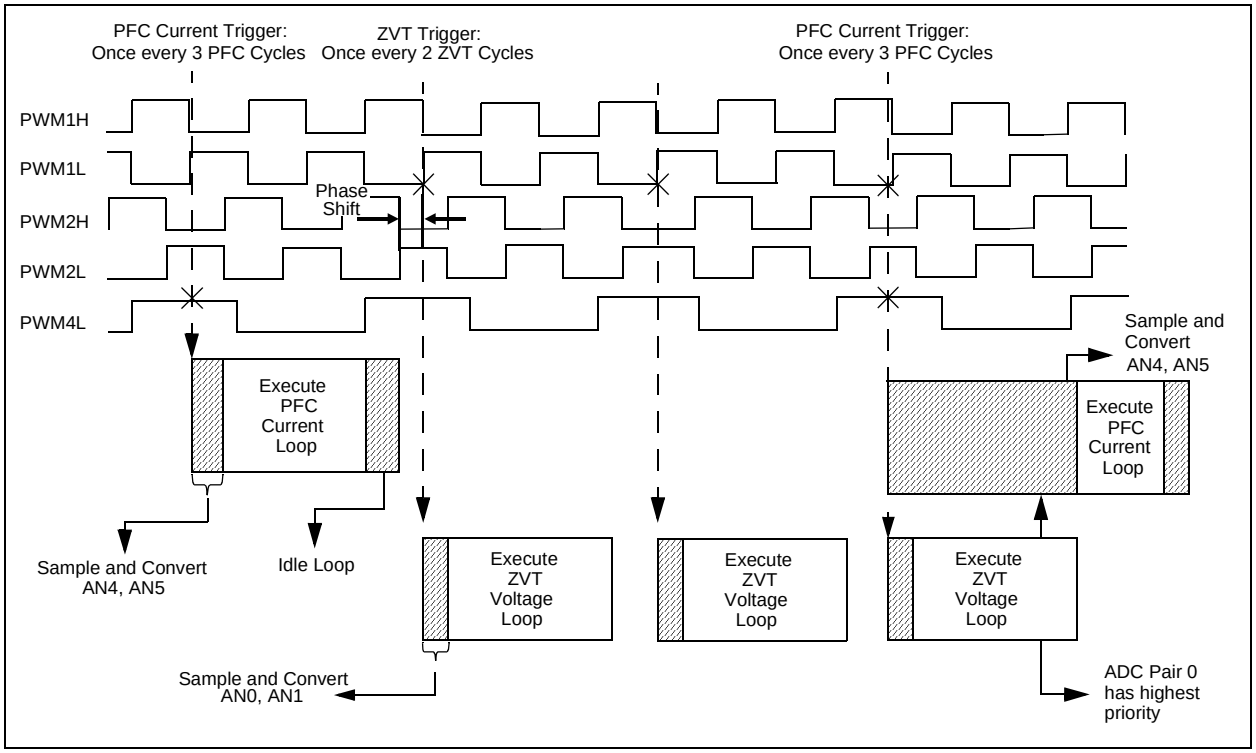
The voltage loop is executed every two PWM periods, but the measured voltage is only updated when data is received by the UART. This UART data reception is asynchronous to the PWM drive signals.

3.3.3 Primary Side Software Time Management

Both the PFC and ZVT converters are controlled using a single dsPIC DSC. The execution rates are carefully chosen to effectively utilize the available processing bandwidth of the dsPIC DSC. The flexible PWM-ADC trigger feature of the dsPIC33FJ16GS504 enables precise sampling of analog signals and interleaved control loop execution.

Figure 3-9 shows the interleaved control loop execution as implemented on the primary side control software on the SMPS AC/DC Reference Design.

FIGURE 3-9: INTERLEAVED CONTROL LOOP EXECUTION



3.4 SECONDARY SIDE CONTROL SOFTWARE (DC_DC)

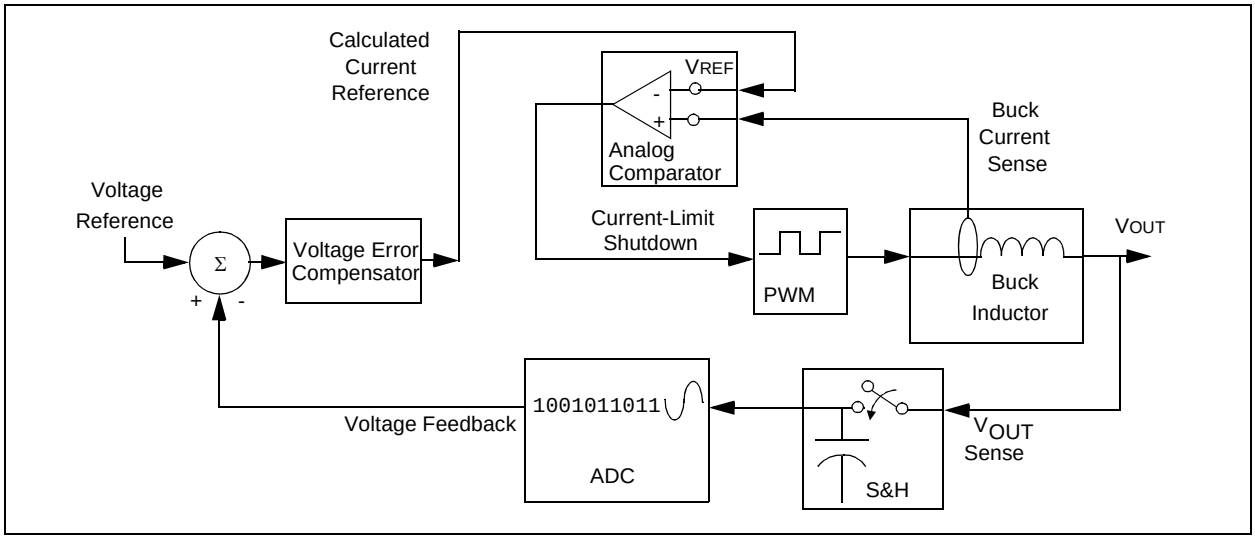
3.4.1 Single-Phase Buck Converter

3.4.1.1 SINGLE-PHASE BUCK CONVERTER CONTROL SCHEME

The Single-Phase Buck Converter on the SMPS AC/DC Reference Design uses peak current mode control. The control scheme is shown in Figure 3-10.

The control loop is implemented by utilizing the analog comparator module. The Buck MOSFET current is sensed using a current transformer and fed directly to the analog comparator input.

FIGURE 3-10: SINGLE-PHASE BUCK CONVERTER CONTROL SCHEME



The measured output voltage is compared with the reference to produce the voltage error. The voltage error compensator is then executed and a current reference value is obtained. The current control loop is implemented on the dsPIC DSC using the analog comparator by varying the programmable threshold in software.

The analog comparators on the dsPIC33FJ16GS504 have built-in programmable Digital-to-Analog Converters (DACs) that determine the comparator threshold. The calculated current reference is used to set a new threshold for the analog comparator.

When the inductor current signal exceeds the programmed threshold, the comparator terminates the PWM pulse. This termination of the PWM pulse effectively modifies the ON time for the PWM signal to control the output voltage.

The Voltage Error Compensator is implemented as a PI function in the ADC ISR.

3.4.1.2 SINGLE-PHASE BUCK CONVERTER IMPLEMENTATION USING THE dsPIC DSC

The resources used on the secondary side dsPIC DSC for the Single-Phase Buck Converter are summarized in Table 3-4.

TABLE 3-4: dsPIC® DSC RESOURCE ALLOCATION FOR SINGLE-PHASE BUCK CONVERTER

Description	Type of Signal	dsPIC® DSC Resource Used
Buck Current	Analog Comparator Input	CMP1A, AN0
Buck Voltage (VOUT)	Analog Input	AN1
Single-Phase Synchronous Buck Gate Drive	Drive Output	PWM4H, PWM4L

The output voltage is measured using the analog input AN1. The analog comparator input CMP1A is connected to the output of the current transformer. The output voltage is controlled by varying the duty cycle of PWM4.

The PWM4 pair is operated in Complementary mode with dead time. The switching frequency is approximately 500 kHz. The duty cycle is controlled directly by the built-in Cycle-by-Cycle Current-Limit mode and the analog comparator.

When the current-sense signal at the input of the analog comparator exceeds the programmed comparator threshold, the PWM output is immediately terminated for the remainder of the PWM cycle.

The Single-Phase Buck Converter circuitry is designed to operate in continuous conduction mode at load currents greater than approximately 3A. If the Single-Phase Buck Converter is operated in Discontinuous Conduction mode, the freewheeling MOSFET is disabled through software.

At no load and light load current (< 3A), the PWM output may enter a "burst" mode. This is caused by a low demand for load current by the converter in this range load current.

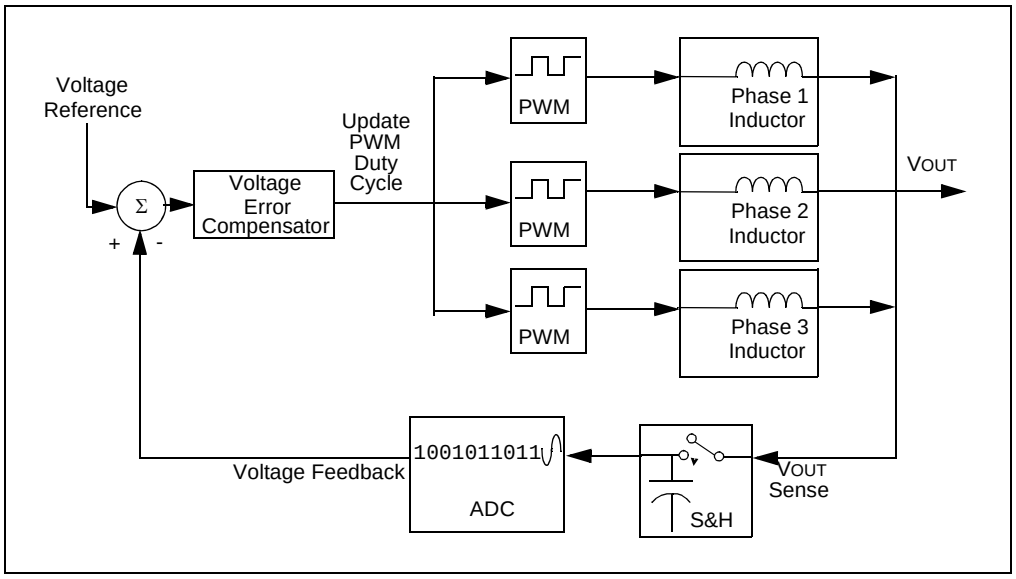
The voltage control loop is executed in the ADC ISR every two PWM cycles.

3.4.2 Multi-Phase Buck Converter

3.4.2.1 MULTI-PHASE BUCK CONVERTER CONTROL SCHEME

Voltage mode control is used for controlling the output of the Multi-Phase Buck Converter on the SMPS AC/DC Reference Design. As shown in Figure 3-11, the control scheme only implements a single control loop.

FIGURE 3-11: MULTI-PHASE BUCK CONVERTER CONTROL SCHEME

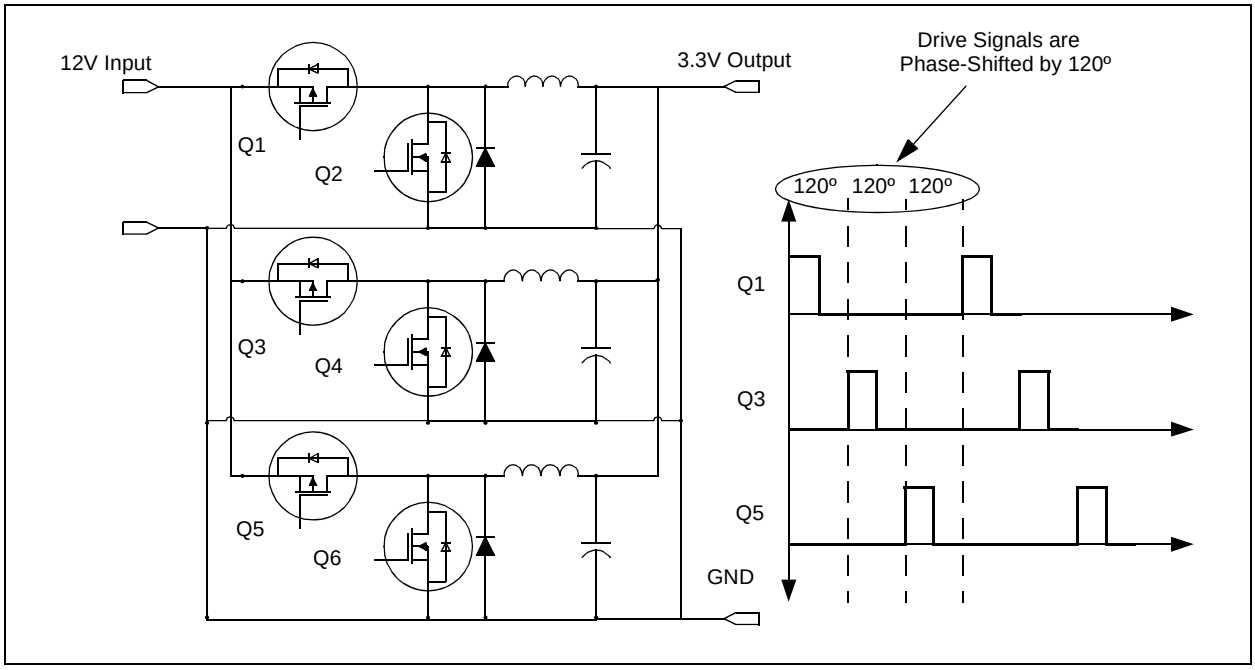


The output voltage is compared with the reference and results in a voltage error, which is fed as an input to the voltage error compensator. The output of the voltage error compensator modifies the duty cycle of all phases of the Multi-Phase Buck Converter.

The voltage error compensator is implemented as a PID function that is implemented in the ADC ISR.

The Multi-Phase converter comprises of three individual phases, but the output is controlled by a single duty cycle that identically drives the three phases. The PWM drive signals for each phase are phase shifted by 120 degrees using the built-in PWM phase-shifting feature available on the dsPIC33FJ16GS504. The PWM drive signals for the Multi-Phase Buck Converter are shown in Figure 3-12.

FIGURE 3-12: MULTI-PHASE BUCK CONVERTER PWM DRIVE SIGNALS



3.4.2.2 MULTI-PHASE BUCK CONVERTER IMPLEMENTATION USING THE dsPIC DSC

Table 3-5 summarizes the resource allocation for the Multi-Phase Buck Converter.

TABLE 3-5: dsPIC® DSC RESOURCE ALLOCATION FOR MULTI-PHASE BUCK CONVERTER

Description	Type of Signal	dsPIC® DSC Resource Used
Buck 1 Current	Analog Comparator Input	CMP2A
Buck 2 Current	Analog Comparator Input	CMP3A
Buck 3 Current	Analog Comparator Input	CMP4A
Buck Voltage	Analog Input	AN3
Multi-Phase Synchronous Gate Drive	Drive Outputs	PWM1H, PWM1L, PWM2H, PWM2L, PWM3H, PWM3L

The output voltage is measured from the analog input AN3. As this converter uses voltage mode control, there is no need for current measurement. However, overcurrent protection must be provided for each individual phase. Overcurrent protection is implemented using the analog comparators on the dsPIC33FJ16GS504. CMP2A, CMP3A and CMP4A are used for the overcurrent sensing for the Multi-Phase Buck Converter.

Each of the three phases is driven by a pair of complementary PWM signals. The PWM module on the dsPIC33FJ16GS504 provides a built-in mode to generate a pair of complementary PWM outputs with dead time insertion. The PWM module also has a feature to generate a Master Period and Master Duty Cycle for multiple outputs. PWM1, PWM2, and PWM3 are all configured for a PWM switching frequency of approximately 500 kHz, and complementary mode operation with dead time.

PWM2 is phase advanced by 120 degrees from PWM1, and PWM3 is phase advanced by 120 degrees from PWM2 (or 240 degrees from PWM1). The voltage control loop is executed every two PWM cycles. The control loop is called from the ADC ISR.

The output of the voltage control loop is used to directly modify the PWM Master Duty Cycle to control the output voltage.

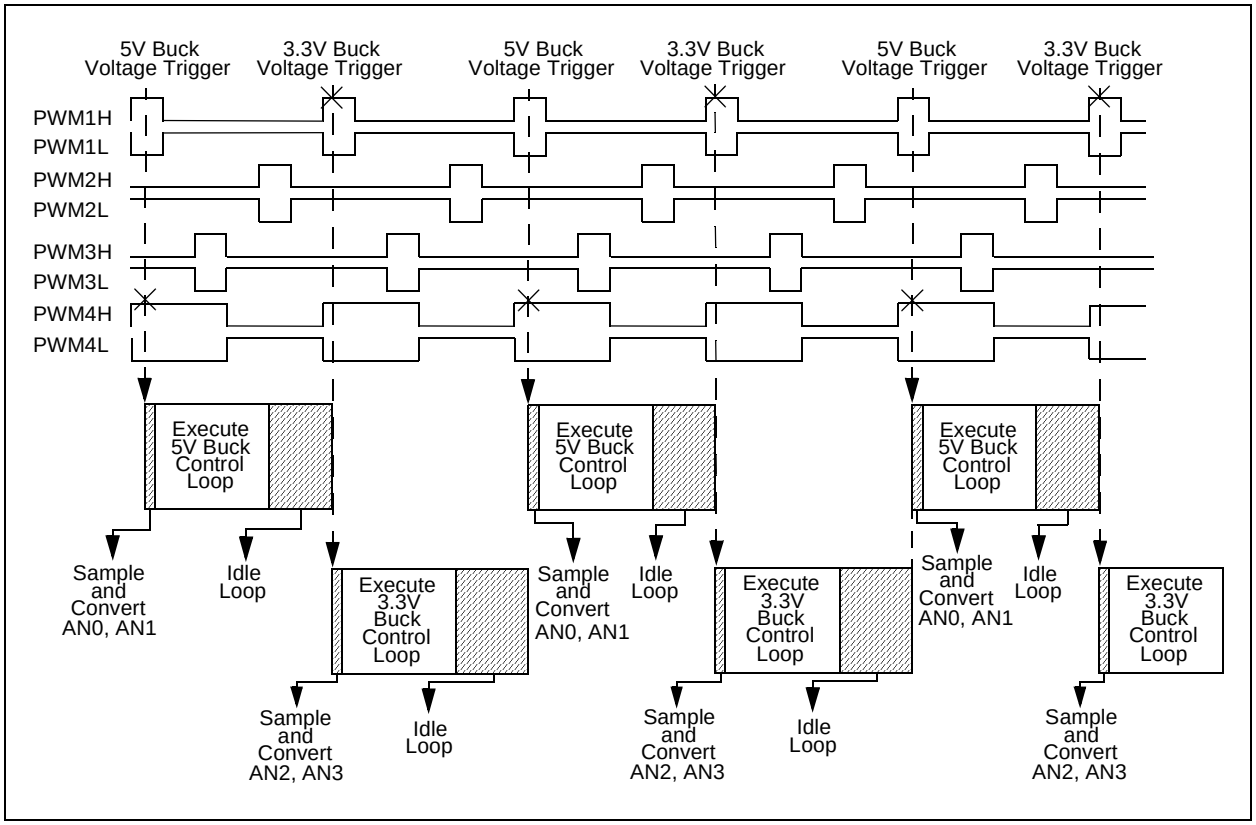
3.4.3 Secondary Side Software Time Management

The Single-Phase Buck Converter and Multi-Phase Buck Converter are both controlled digitally by the same dsPIC DSC. Both converters operate at the same switching frequency.

The two control loops are executed in an interleaved manner as shown in Figure 3-13. The execution rate for each control loop is once every other PWM cycle. The execution rate is determined by the execution times of each control loop.

The ADC ISR assumes the highest priority of all user software. Other interrupts are assigned lower priority than the ADC interrupt, and all auxiliary software functions are performed in the "Idle loop" (when the ADC interrupt is not being serviced).

FIGURE 3-13: INTERLEAVED CONTROL LOOP EXECUTION FOR SINGLE-PHASE AND MULTI-PHASE BUCK CONVERTERS



3.5 AUXILIARY SOFTWARE ROUTINES

3.5.1 Output Sequencing

Many applications require specific turn-on and turn-off sequencing of power supplies to ensure correct operation of the downstream electronics. The SMPS AC/DC Reference Design implements power-on sequencing in the following order:

1. Initial start-up delay (allows all circuitry to stabilize after power-up).
2. PFC Converter ramps to around 420V.
3. Phase-Shift ZVT Converter ramps to 12V.
4. Single-Phase Buck Converter ramps to 5V.
5. Multi-Phase Buck Converter ramps to 3.3V.

3.5.2 Soft-Start Routine

Each individual stage of the SMPS AC/DC Reference Design employs a controlled soft-start routine. At power-up, all reference set points are configured to produce 0V output. Once the power-on delay has lapsed, the outputs begin their soft-start where the reference set point is incremented until the desired output voltage is reached.

3.5.3 Overtemperature Protection

Temperature sensors are provided on the SMPS AC/DC Reference Design in two positions. Overtemperature protection must be enabled to prevent damage to the system in the event of:

- Insufficient airflow in the system caused by a failure of the cooling fan
- Operation of the system at a high ambient temperature

The implementation detail for each sensor is described in the following sections.

3.5.3.1 PCB OVERTEMPERATURE PROTECTION

One of the PCB temperature sensors is located on the secondary side in the middle of the four Buck phases. The other temperature sensor is located on the primary side just below the Boost inductor (L4). An analog temperature sensor is chosen that outputs an analog voltage proportional to the measured temperature.

The output of the temperature sensor is connected to analog input AN8 on the secondary side dsPIC DSC, and AN10 on the primary side dsPIC DSC. The PCB temperature is measured in the ADC ISR and checked for overtemperature protection in the fault loop. The maximum temperature set point is configured to approximately 90°C. If the measured temperature exceeds the maximum set point, a fault is generated and the PWM outputs are turned OFF.

3.5.4 Input AC Undervoltage/Overvoltage Protection

The PFC Boost Converter is designed to operate normally for input voltages in the range 85V–265V. In the event of an undervoltage condition, the circuit components will undergo excessive stress due to the additional current drawn by the system to deliver maximum output power. Therefore, undervoltage and overvoltage faults must be implemented to prevent damage to the system and load. In the event of an overvoltage condition, the input voltage may exceed the device ratings.

There are instances when the power grid may exhibit momentary voltage fluctuations, which must be ignored by the system.

The input AC voltage protection is implemented in software by calculating the average input voltage in the ADC ISR. The average input voltage is calculated as a part of the PFC control scheme, and is checked in the fault loop to detect a sustained undervoltage/overvoltage condition.

The first time an undervoltage/overvoltage condition is detected, a counter is incremented. If the undervoltage/overvoltage condition remains for an extended period of time, a fault is generated and the outputs are turned OFF.

3.5.5 Fault Source Identification

If a Fault condition is detected, it is often required that the system be turned OFF to prevent damage. The PWM module on the dsPIC33FJ16GS504 has a built-in latched fault mode. Using the latched fault mode, certain faults will immediately disable the PWM outputs with no software overhead.

Each fault is assigned a fault ID to indicate the source of the last fault that occurred. A visual indication is also provided using LEDs on both the primary and secondary side of the SMPS AC/DC Reference Design.

The LED flashes the same number of times as the fault ID of the source that caused the fault. The source of the fault can be decoded using the values in Table 3-6 and Table 3-7.

TABLE 3-6: FAULT SOURCE INDICATION ON PRIMARY SIDE

Fault ID	Source of Fault
1	PCB overtemperature
2	PFC output overvoltage
3	ZVT overcurrent
4	AC overvoltage
5	AC undervoltage
6	Secondary UART failure
7	System overload

TABLE 3-7: FAULT SOURCE INDICATION ON SECONDARY SIDE

Fault ID	Source of Fault
1	12V Buck overvoltage
2	12V Buck undervoltage
3	Multi-phase overcurrent
4	PCB overtemperature
5	Single-phase overcurrent

Chapter 4. System Operation

This chapter describes the system setup and operation of the SMPS AC/DC Reference Design.

4.1 SYSTEM SETUP

4.1.1 Recommended Test Equipment

The following list of test equipment is recommended for complete evaluation of the SMPS AC/DC Reference Design and/or development of software.

- Oscilloscope
- High Voltage Probe (100:1 attenuation ratio) or Differential Probe
- 10A AC Current Probe
- Power Quality Meter
- DC Electronic Load (350W or higher, and should have capability to load at least two outputs simultaneously)
- 0V-265V Variac or Programmable AC Source (500W or higher)
- Two Digital Multimeters

4.1.2 Functional Blocks of the System

Figure 4-1 shows a block diagram of the SMPS AC/DC Reference Design. Table 4-1 describes the inputs and outputs of the system and also displays the location of the isolation barrier. To assist in identifying each functional block on the SMPS AC/DC Reference Design, Figure 4-2 shows a top-view of the system with each block called out with dotted lines.

FIGURE 4-1: SMPS AC/DC REFERENCE DESIGN BLOCK DIAGRAM

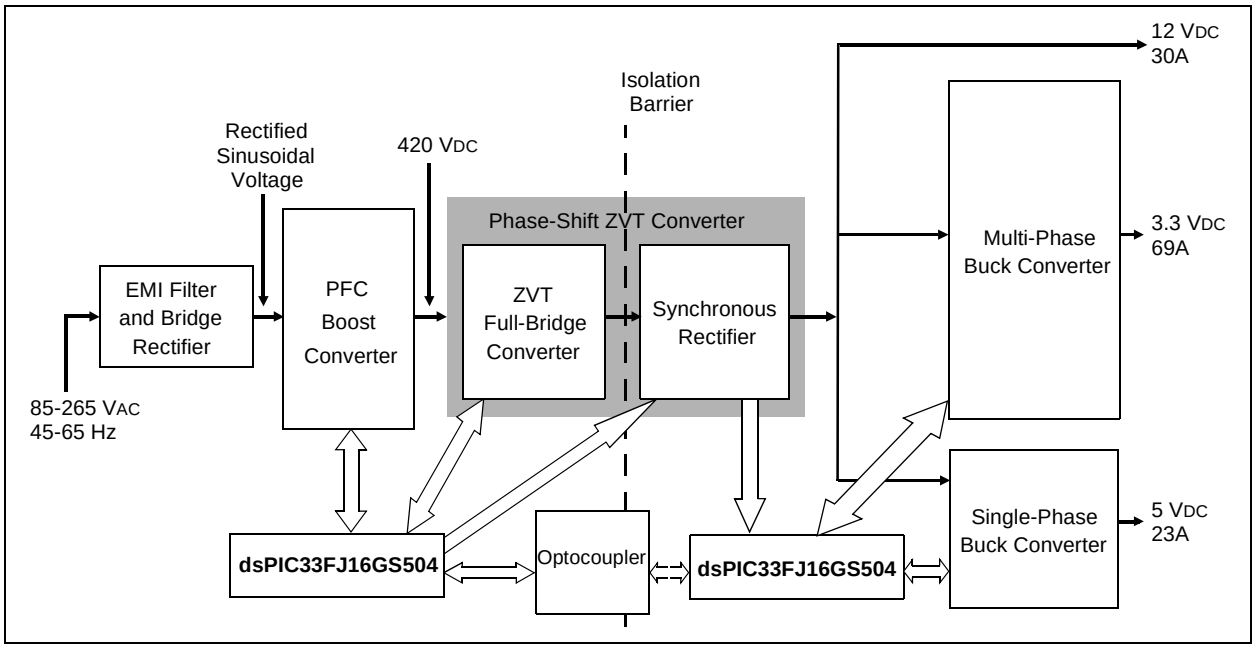
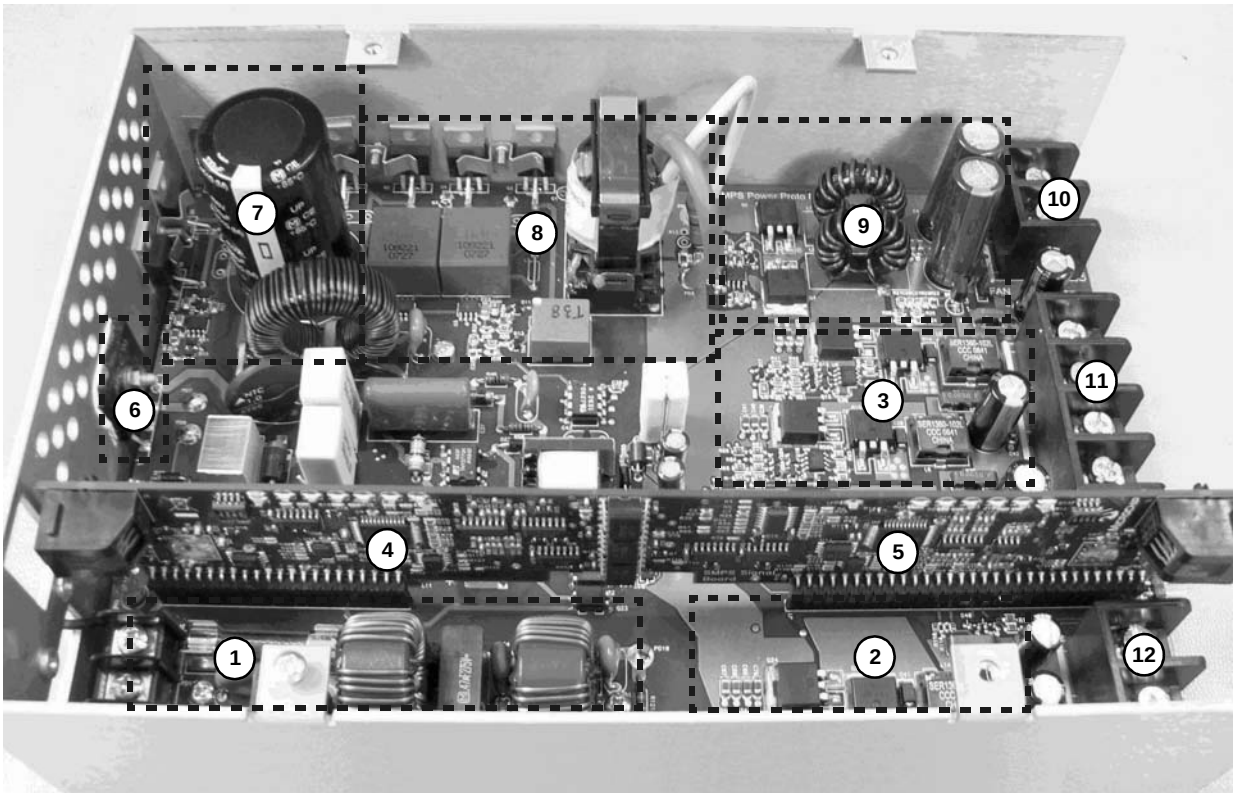


FIGURE 4-2: FUNCTIONAL BLOCKS OF SMPS AC/DC REFERENCE DESIGN



1. EMI Filter
2. Single-Phase Converter
3. Multi-Phase Converter
4. Primary Side Controller
5. Secondary Side Controller
6. Bridge Rectifier
7. PFC Boost Converter
8. ZVT Full-Bridge Converter
9. Synchronous Rectifier
10. 12V Output (Intermediate Bus)
11. 3.3V Output
12. 5V Output

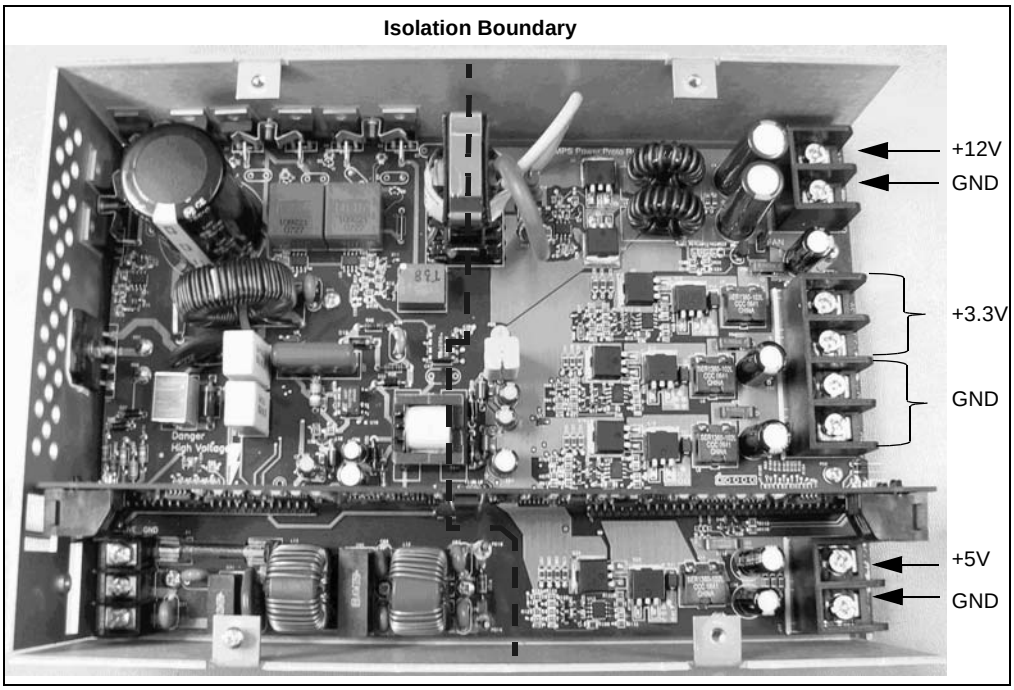
TABLE 4-1: INPUT AND OUTPUT ELECTRICAL SPECIFICATIONS

Functional Block	Input	Output
EMI Filter	85-265V AC, 45-65 Hz	85-265V AC, 45-65 Hz
Bridge Rectifier	85-265V AC, 45-65 Hz	120-374V DC (unregulated)
PFC Boost Converter	120-374V DC (unregulated)	420V DC
Full-Bridge Converter	420V DC	N/A
Synchronous Rectifier	N/A	12V DC
Multi-Phase Buck Converter	12V DC	3.3V DC
Single-Phase Buck Converter	12V DC	5V DC

4.1.3 Safety Isolation Information

The SMPS AC/DC Reference Design provides safety isolation to protect users and downstream electronics from the input AC Mains voltage. The location of the isolation boundary on the SMPS AC/DC Reference Design is displayed with a dotted line in Figure 4-3.

FIGURE 4-3: ISOLATION BOUNDARY ON SMPS AC/DC REFERENCE DESIGN



NOTICE

During testing and evaluation of the SMPS AC/DC Reference Design, no equipment should be connected across the isolation boundary. This applies to oscilloscope probes, multimeters, and programmers/debuggers. Under no circumstances should the Live_GND (on the primary or "live" side) and GND (on the secondary or "isolated" side) be tied together.

As a general rule, the primary (live) side and the secondary (isolated) side should always be tested independently with no connections across the isolation boundary.

Before connecting oscilloscope probes to the SMPS AC/DC Reference Design, ensure that the oscilloscope is isolated from the SMPS AC/DC Reference Design.

Table 4-2 lists the location where each functional block resides with respect to the isolation barrier.

TABLE 4-2: LOCATION OF FUNCTIONAL BLOCK WITH RESPECT TO ISOLATION BARRIER

Functional Block	Live or Isolated Side?	
	Power Circuit	Control Circuit
EMI Filter	Primary (Live)	N/A
Bridge Rectifier	Primary (Live)	N/A
PFC Boost Converter	Primary (Live)	Primary (Live)
Full-Bridge Converter	Primary (Live)	Primary (Live)
Synchronous Rectifier	Secondary (Isolated)	Primary (Live)
Multi-Phase Buck Converter	Secondary (Isolated)	Secondary (Isolated)
Single-Phase Buck Converter	Secondary (Isolated)	Secondary (Isolated)

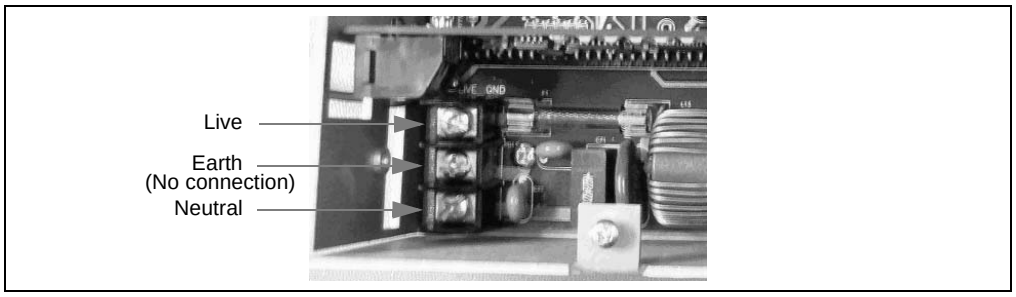
4.1.4 System Connections

4.1.4.1 INPUT CONNECTIONS

The AC input connector (J16) is shown in Figure 4-4. The SMPS AC/DC Reference Design has a transparent lid (not shown in pictures) with a 12V fan mounted on it. There are three holes provided in the lid to fasten the connection screws on the AC input connector (J16).

Ensure that the power chord is not connected to the Variac or programmable AC source (or AC Mains). Connect the AC cord with terminal lugs to the AC input connector in the configuration shown in Figure 4-4.

FIGURE 4-4: SMPS AC/DC REFERENCE DESIGN INPUT CONNECTIONS

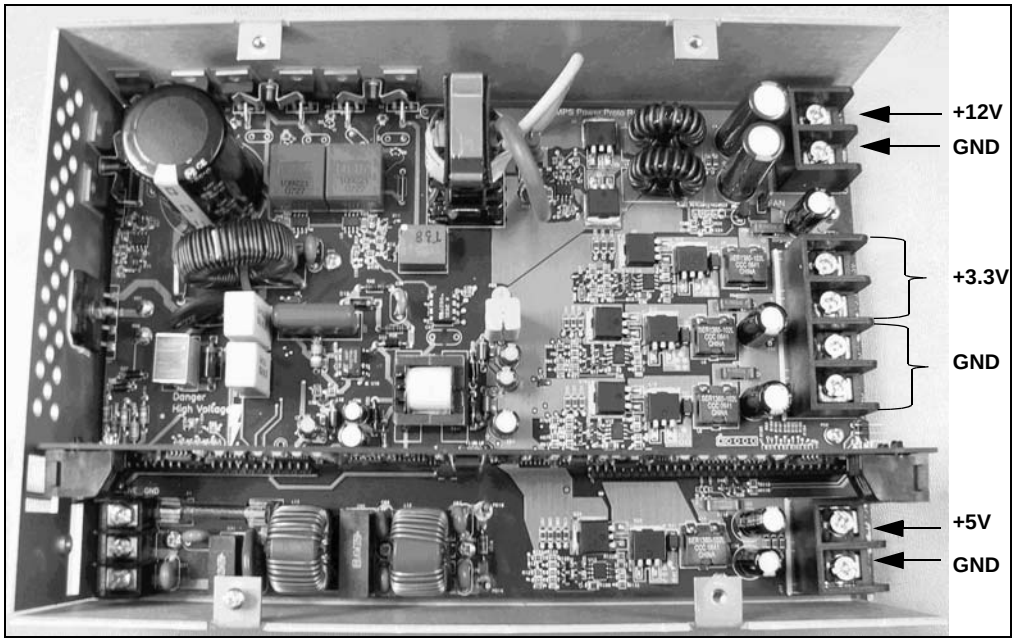


This is the minimum connection required to power up the SMPS AC/DC Reference Design. However, other connections are recommended for detailed testing and evaluation of the system.

4.1.4.2 OUTPUT CONNECTIONS

Ensure that the SMPS AC/DC Reference Design is not powered. Connect DC Electronic Loads (if available) to the 5V and 3.3V output terminals shown in Figure 4-5.

FIGURE 4-5: SMPS AC/DC REFERENCE DESIGN OUTPUT CONNECTIONS



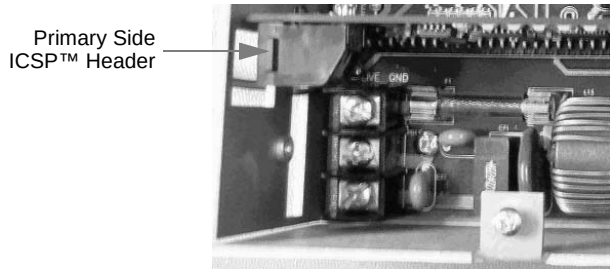
A DC electronic load can be used to adjust the output power delivered by the SMPS AC/DC Reference Design. If a DC electronic load is not available, a rheostat or resistors with sufficient power ratings may also be used for loading the SMPS AC/DC Reference Design.

4.1.4.3 PROGRAMMING CONNECTIONS

The SMPS AC/DC Reference Design comes pre-programmed with the control software and does not require a programmer to be connected to the system. However, ICSP™ headers are provided on the primary and secondary side for software development and testing.

Figure 4-6 shows the location of the primary side programming header (J2 on the control board).

FIGURE 4-6: PRIMARY SIDE PROGRAMMING HEADER

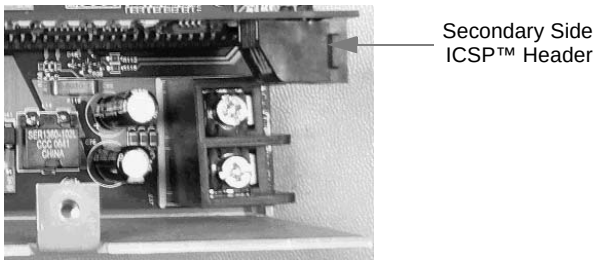


CAUTION

The primary side ICSP header (J2) is not isolated from the AC Mains. An isolated USB hub must be used to connect the programmer to the computer's USB port. If the power supply of the SMPS AC/DC Reference Design is not isolated before programming the device, ensure that the computer is isolated or removed from the grid.

Figure 4-7 shows the location of the secondary side programming header (J1 on the control board).

FIGURE 4-7: SECONDARY SIDE PROGRAMMING HEADER



The secondary side ICSP header is isolated from the AC Mains, so there are no special precautions necessary when programming the device.

4.2 SYSTEM OPERATION

4.2.1 System Power-Up

Once the input and output connections as described in **Section 4.1.4 "System Connections"** are completed, the mains voltage can be applied to the SMPS AC/DC Reference Design.

There are three power-on indicator LEDs on the system. One LED (D38) on the power board near the AC input terminals, and two more on the control board (one on the primary side (LED1), and one on the secondary side (LED2)).

There will be a short delay before the 12V, 5V, and 3.3V outputs are ON because of the soft-start routines and output sequencing scheme implemented on each stage of the SMPS AC/DC Reference Design. Details of the soft-start routine and output sequencing are provided in **Chapter 3. "Software Design"**.

As soon as the 12V output is ON, the cooling fan mounted on the lid will start running. LEDs are provided near each output terminal to indicate that the output is ON.

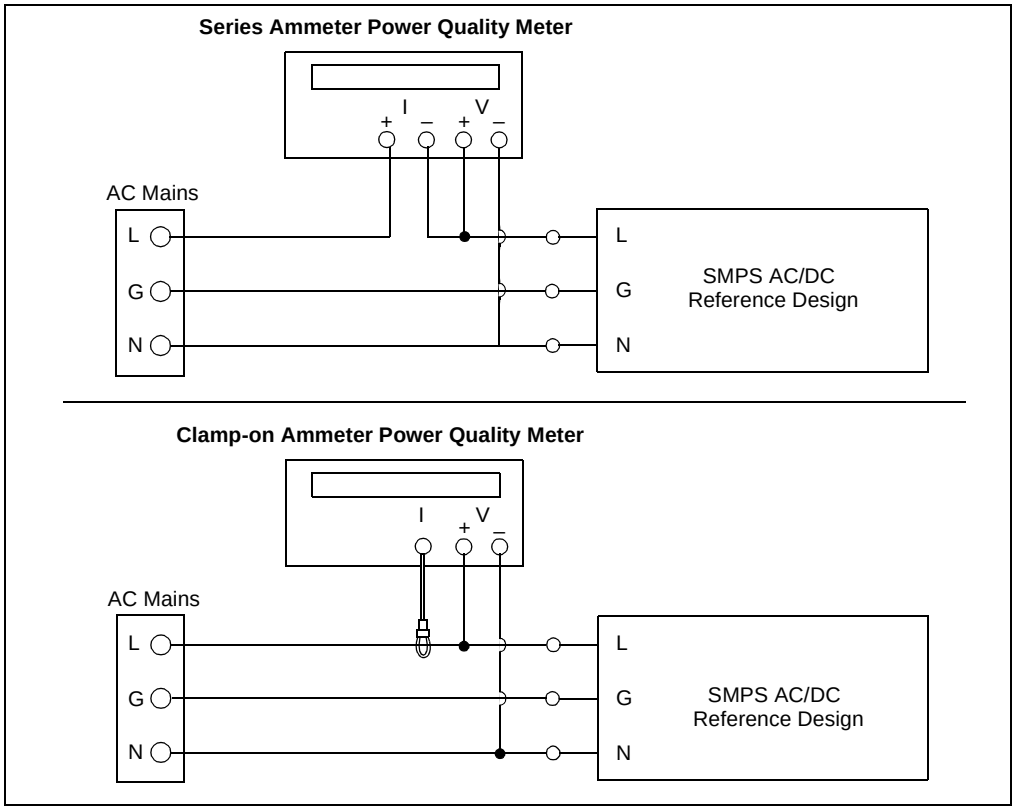
Faults are indicated on the control board with two LEDs (one on the primary side (D34) and one on the secondary side (D33)). Details of faults are provided in **Chapter 3. "Software Design"**.

4.2.2 System Evaluation and Testing

4.2.2.1 INPUT PERFORMANCE TESTING

The input specifications of the SMPS AC/DC Reference Design can be tested by using a power meter. The voltage is measured directly across the Live and Neutral terminals on the SMPS AC/DC Reference Design. The input current is measured by sensing the current through either the Live or Neutral line. Figure 4-8 shows two separate power meter connections depending on the type of power meter used.

FIGURE 4-8: TYPICAL POWER METER CONNECTIONS



A power meter is capable of measuring the input Power Factor of the SMPS AC/DC Reference Design and also the Total Harmonic Distortion (THD) on the current drawn by the system.

Using a programmable AC source will enable the user to evaluate the system performance over the entire range of input voltage (85V-265V, 45Hz-65Hz).

4.2.2.2 OUTPUT PERFORMANCE TESTING

The SMPS AC/DC Reference Design can be loaded using DC electronic loads. A number of output parameters can be tested by connecting oscilloscope probes to the output terminals. Some of the parameters that can be tested are:

- Output Ripple Voltage
- Load Regulation
- Transient Response
- Step-Load Response
- Fault Shutdown Delay

NOTES:

Appendix A. Board Layouts and Schematics

A.1 INTRODUCTION

This appendix contains the schematics and layouts for the SMPS AC/DC Reference Design (Power board and Signal board).

A.2 SMPS AC/DC REFERENCE DESIGN LAYOUT

FIGURE A-1: SMPS AC/DC REFERENCE DESIGN LAYOUT (POWER BOARD)

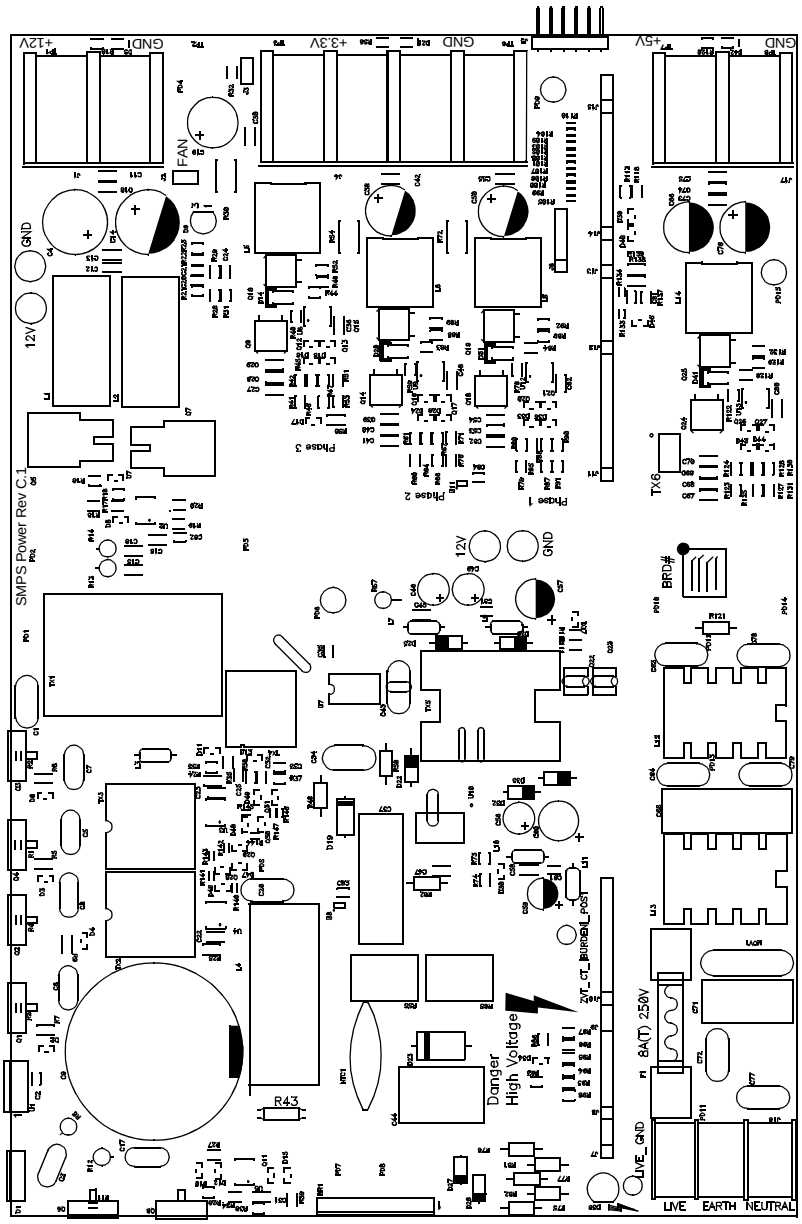
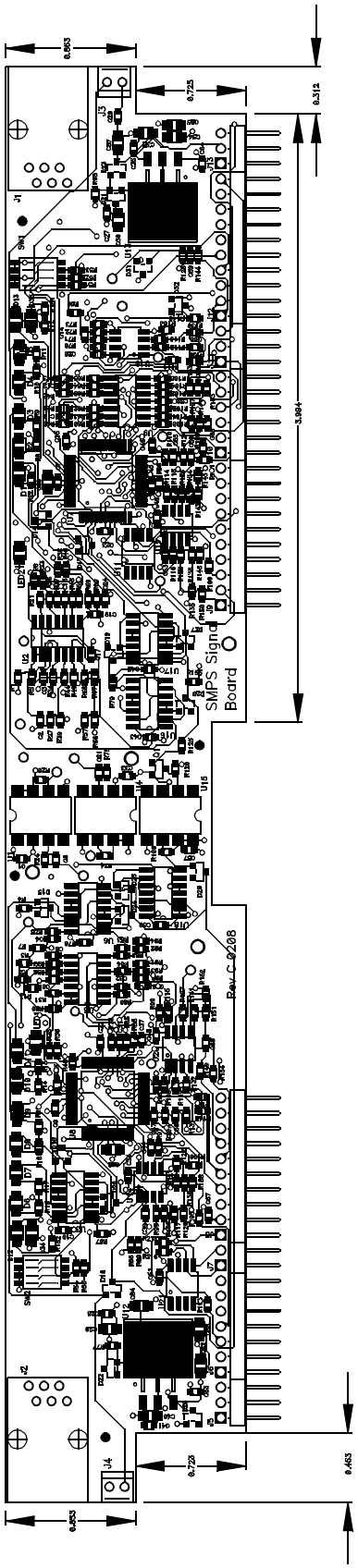


FIGURE A-2: SMPS AC/DC REFERENCE DESIGN LAYOUT (SIGNAL BOARD)



A.3 SMPS AC/DC REFERENCE DESIGN SCHEMATICS

FIGURE A-3: EMI FILTER SCHEMATIC

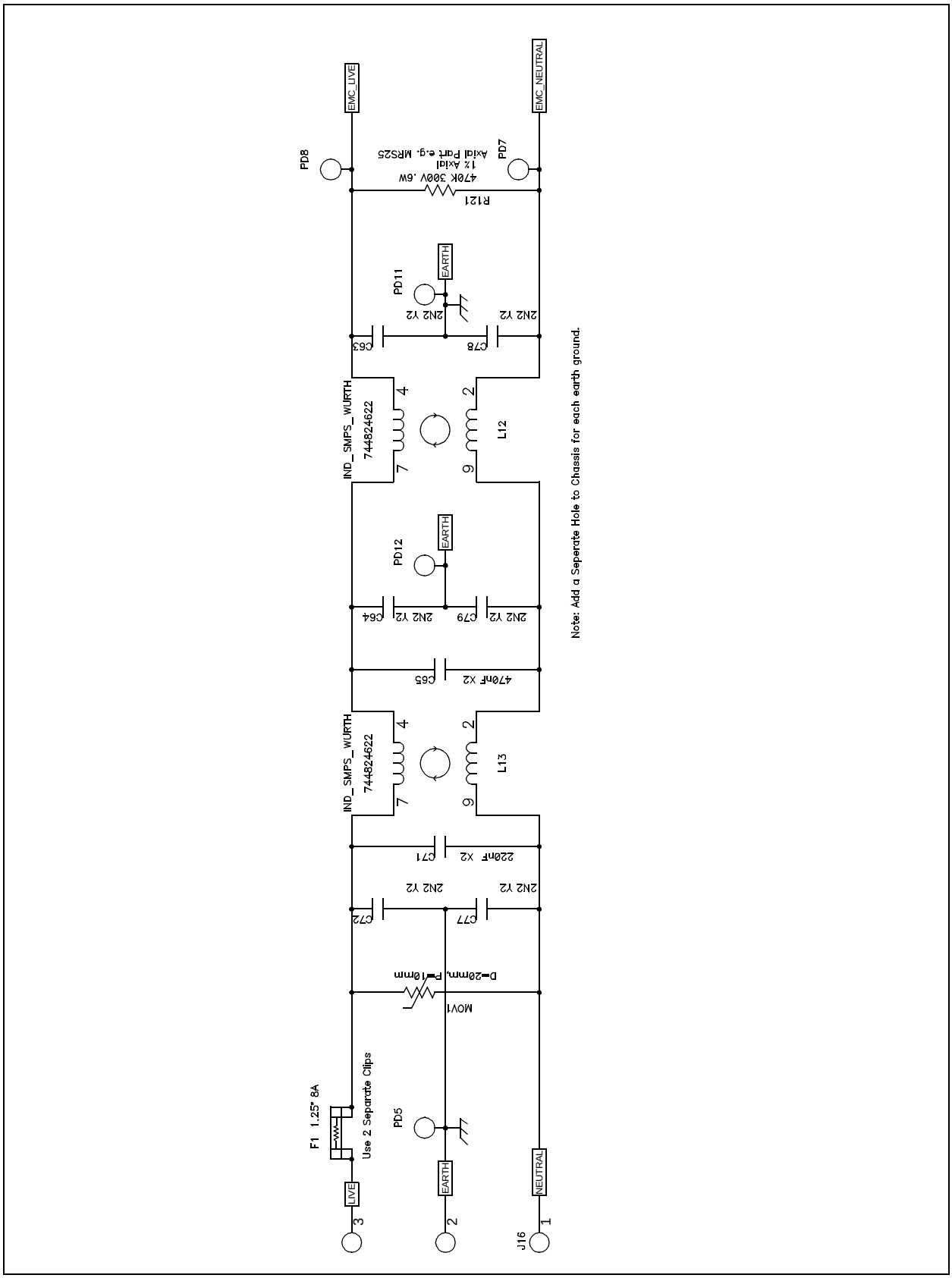


FIGURE A-4: PFC CIRCUIT SCHEMATIC

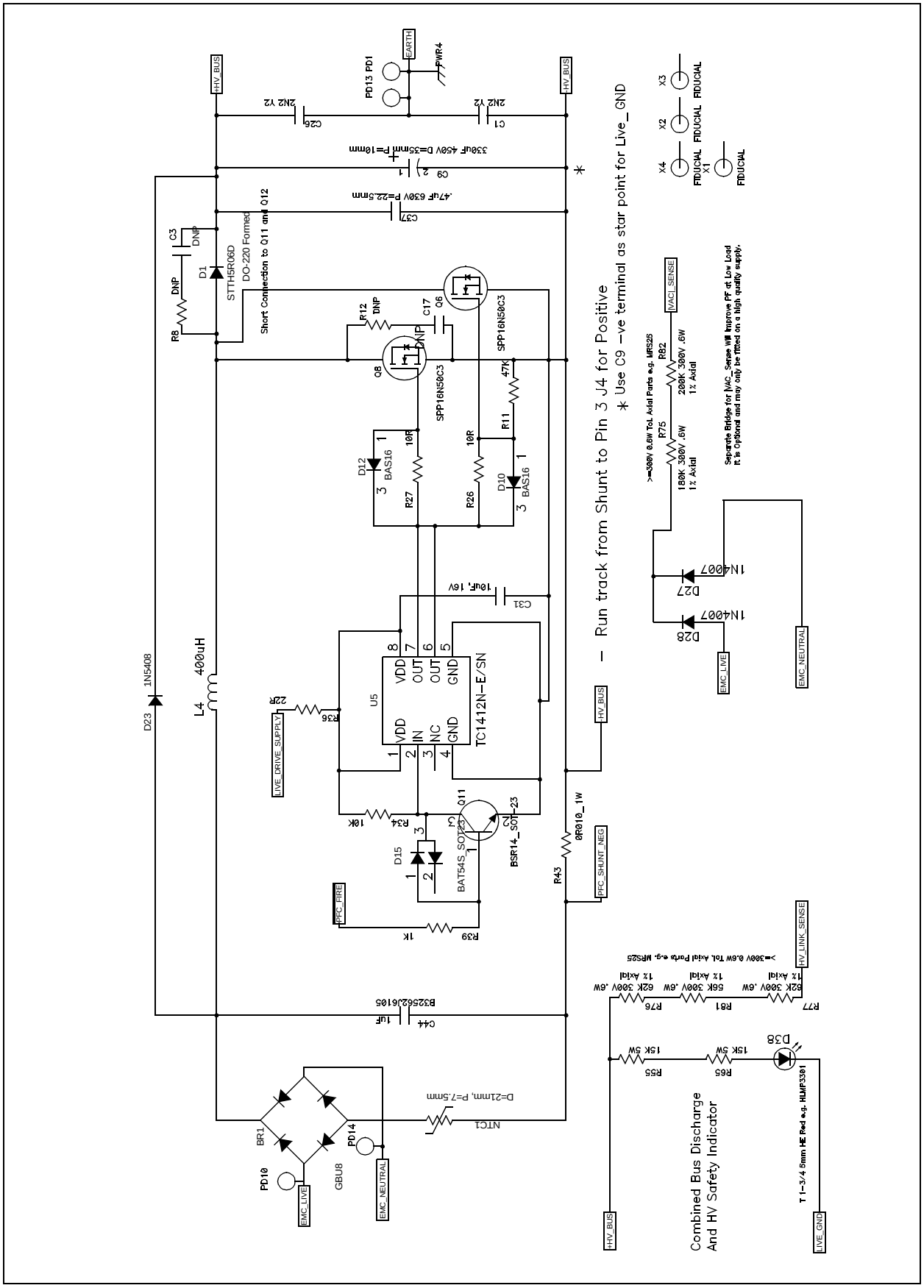


FIGURE A-5: FULL-BRIDGE ZVT SCHEMATIC

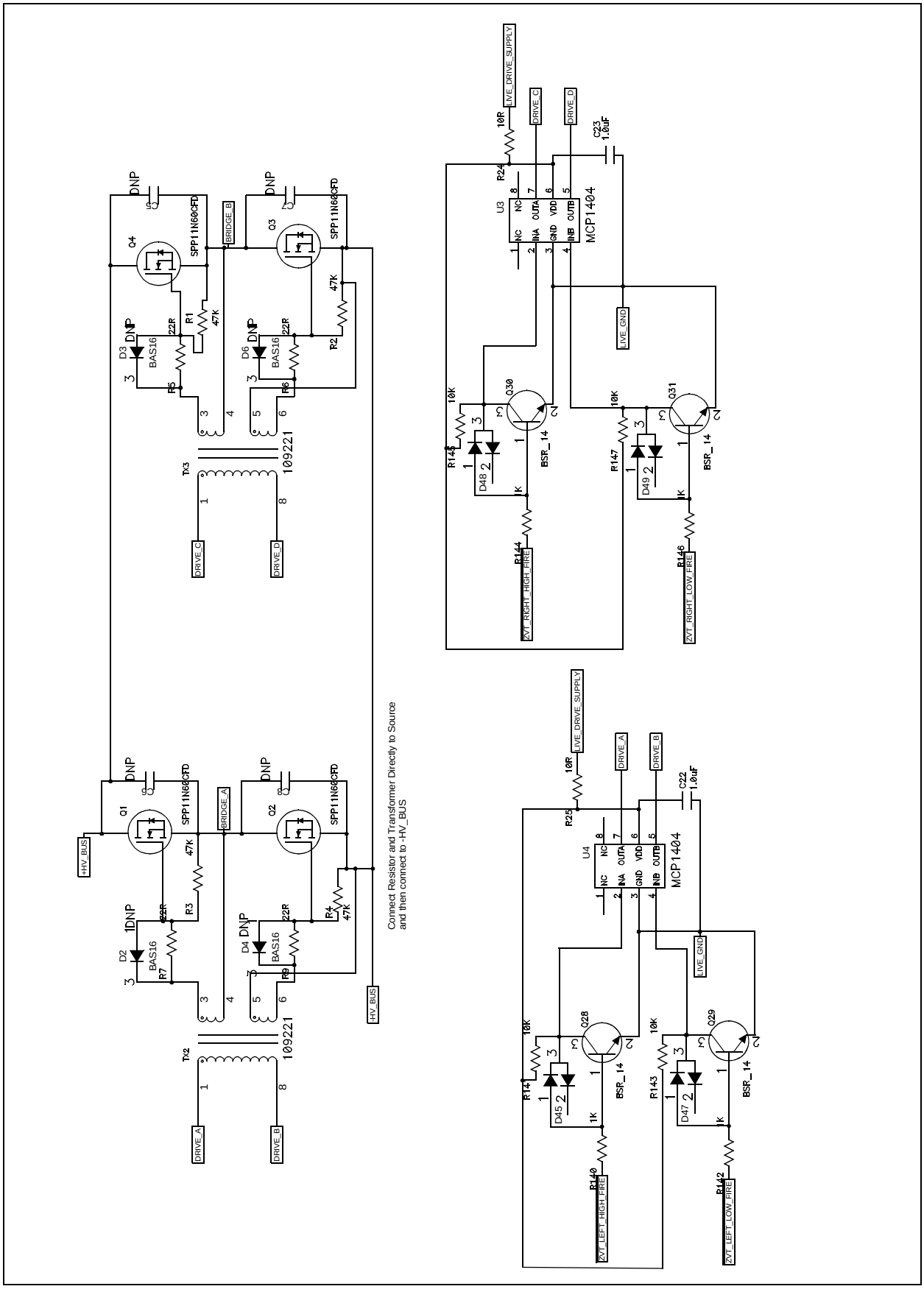


FIGURE A-6: SYNCHRONOUS RECTIFIER AND ZVT CURRENT SENSE SCHEMATIC

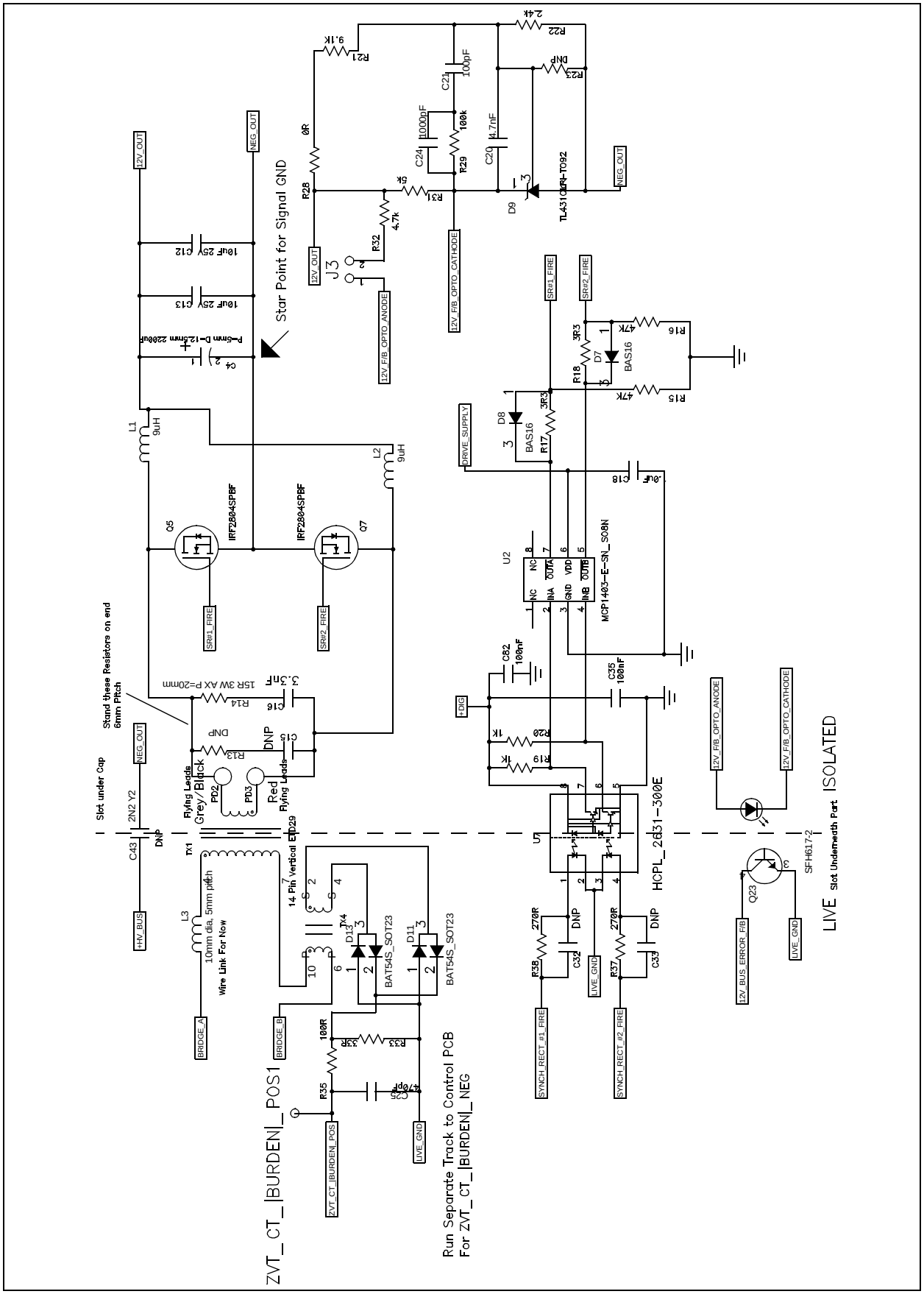


FIGURE A-7: AUXILIARY POWER SUPPLY SCHEMATIC

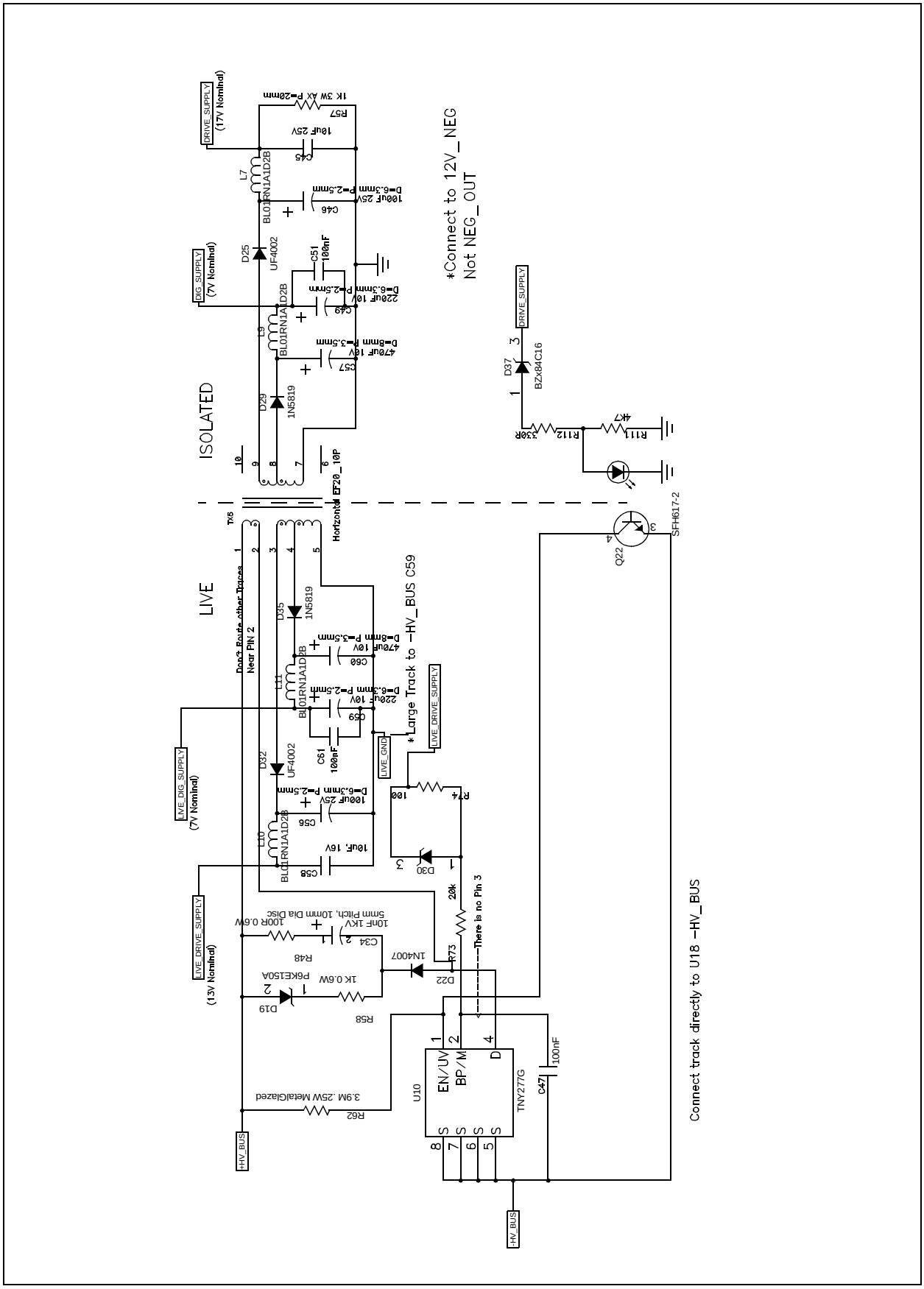


FIGURE A-8: BUCK CONVERTER STAGES SCHEMATIC

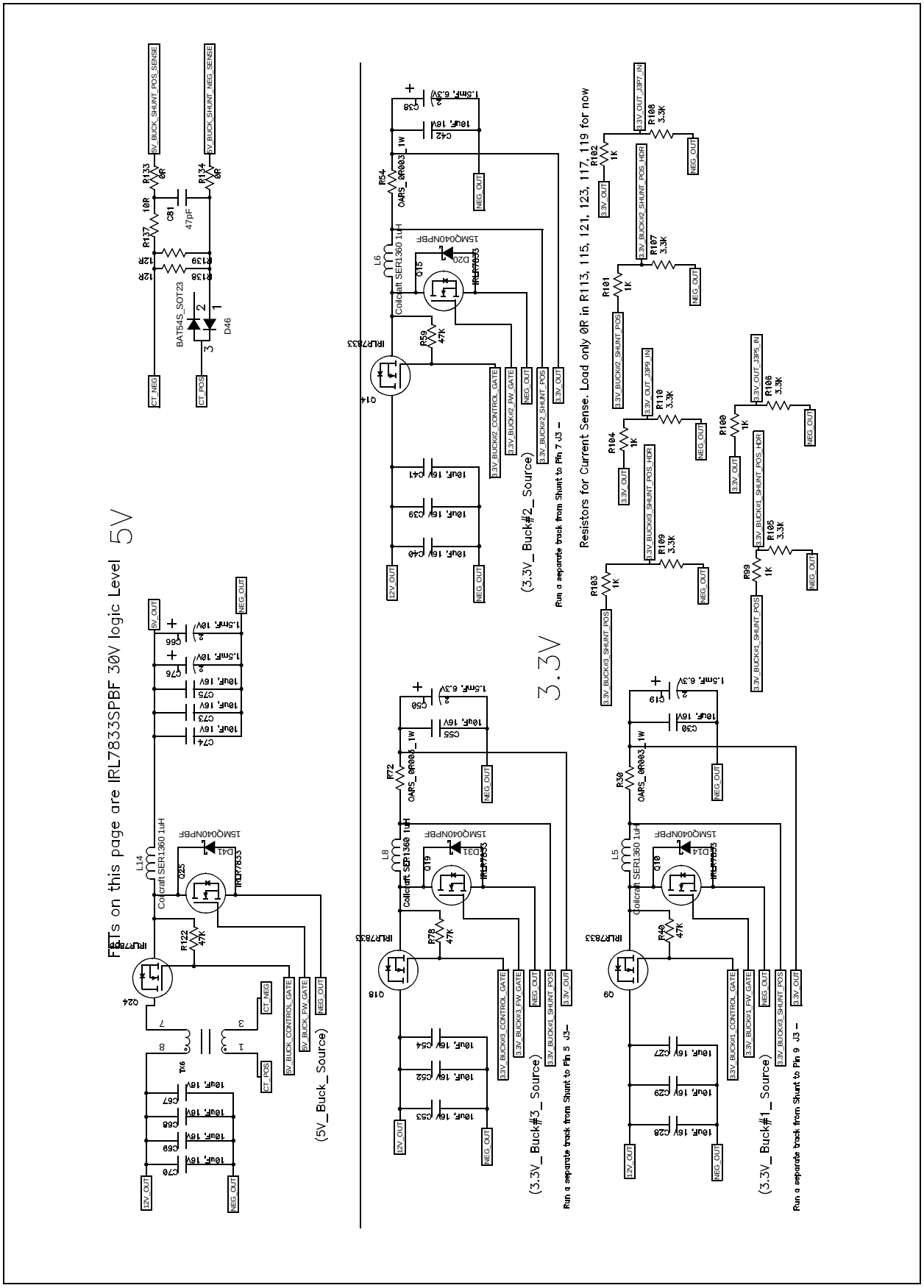


FIGURE A-9: BUCK CONVERTER GATE DRIVE SCHEMATIC

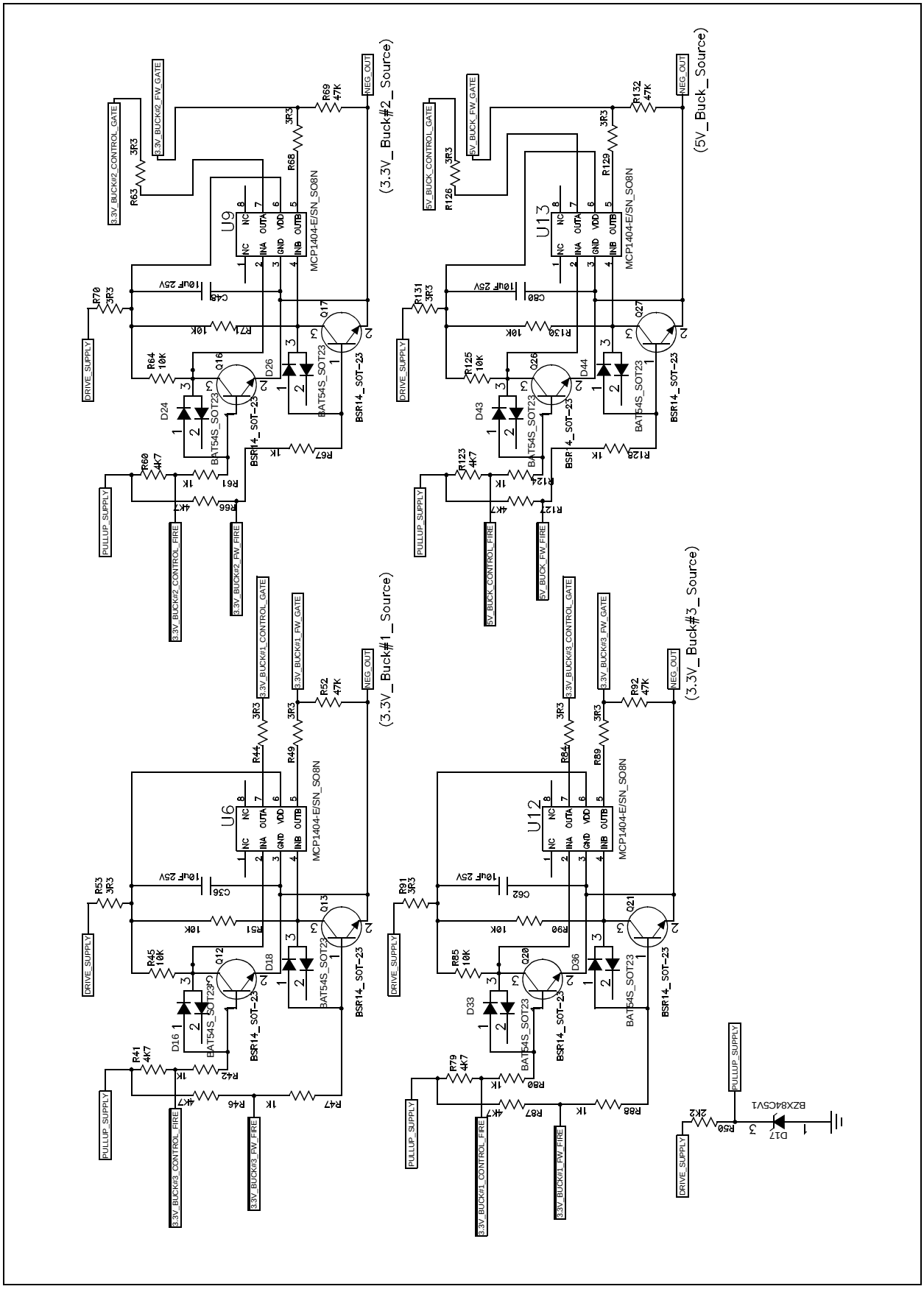


FIGURE A-10: CONTROL BOARD I/F AND TEMPERATURE SENSING/MISC. SCHEMATIC

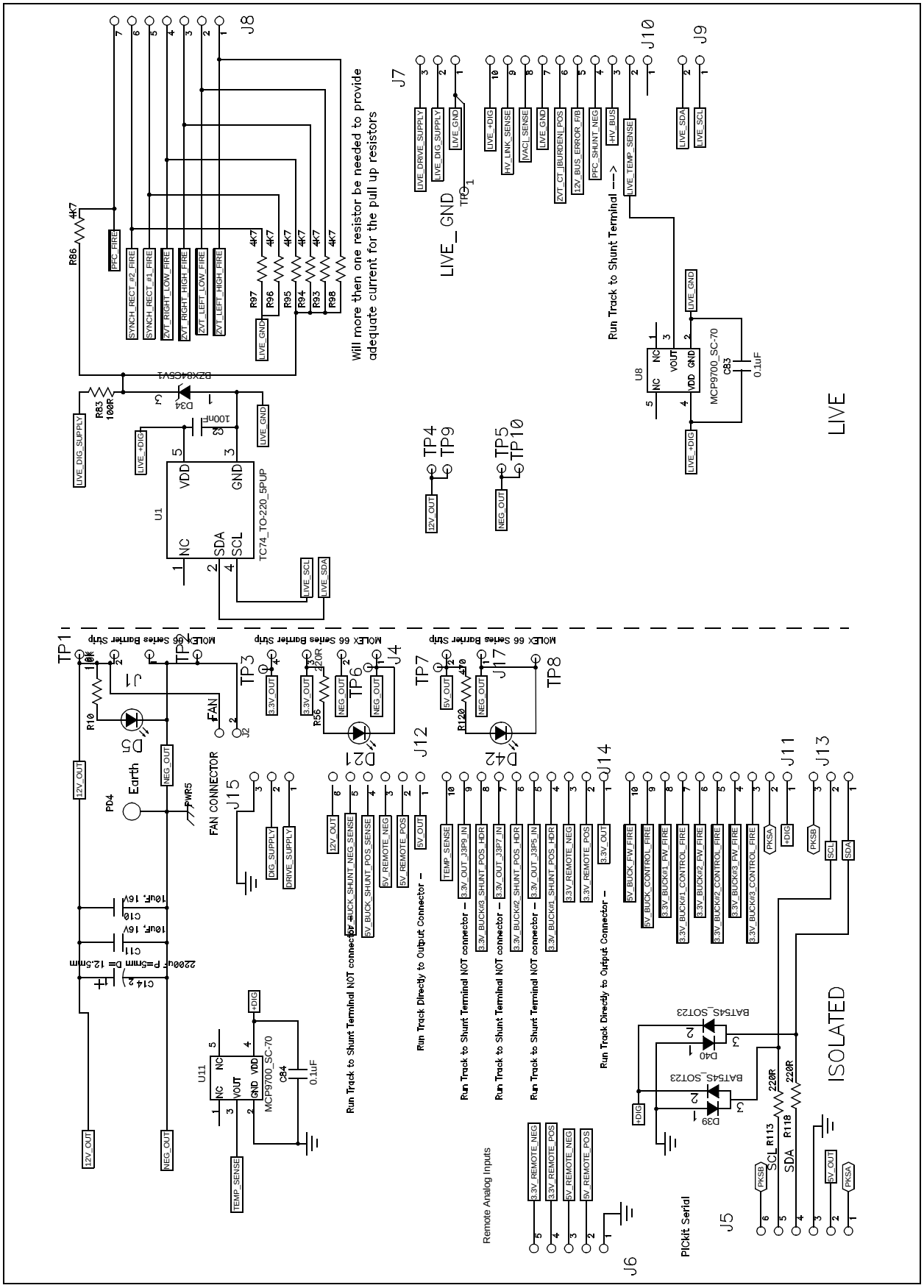


FIGURE A-11: PRIMARY SIDE CONTROLLER SCHEMATIC

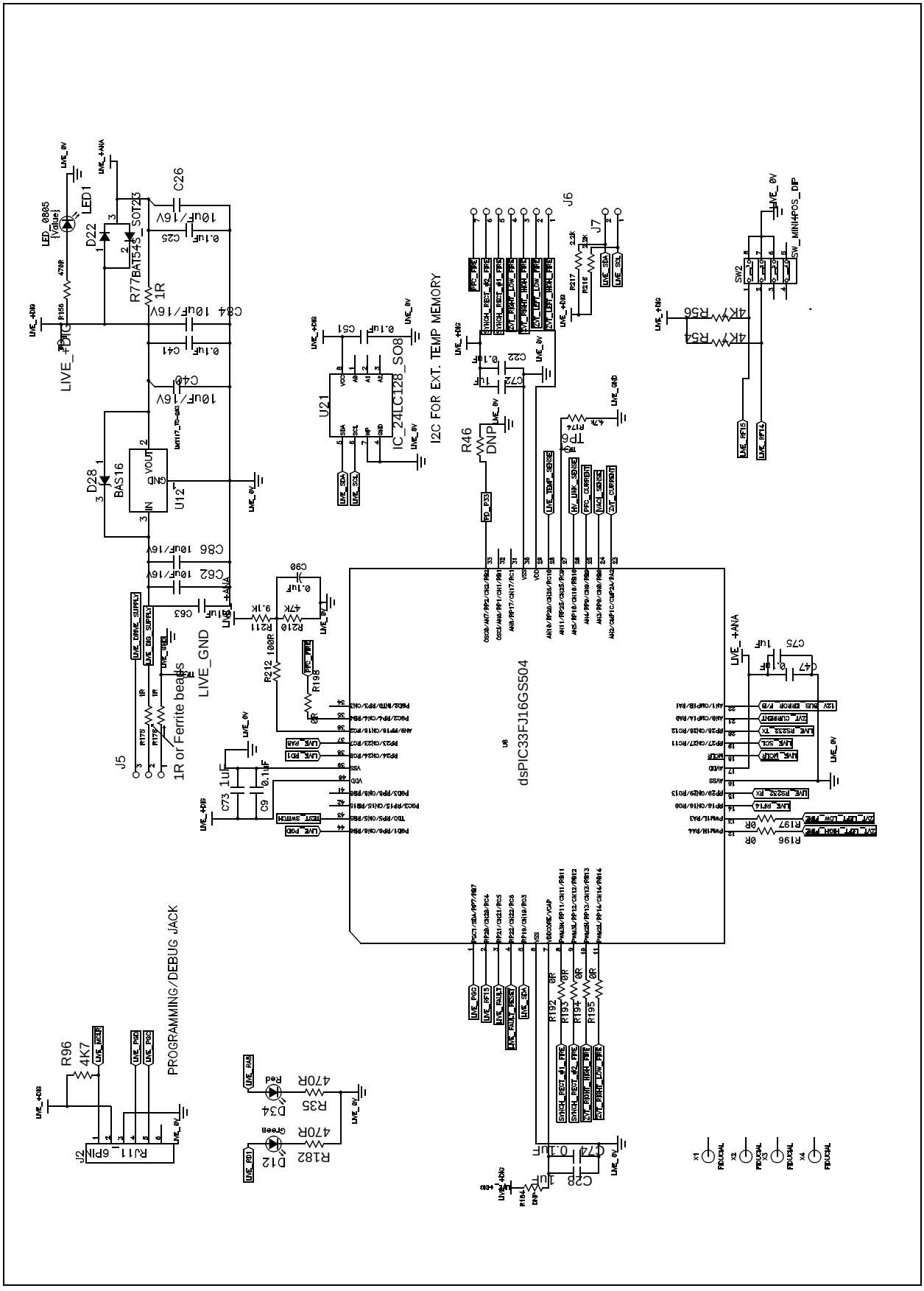


FIGURE A-12: PRIMARY ↔ SECONDARY COMMUNICATION SCHEMATIC

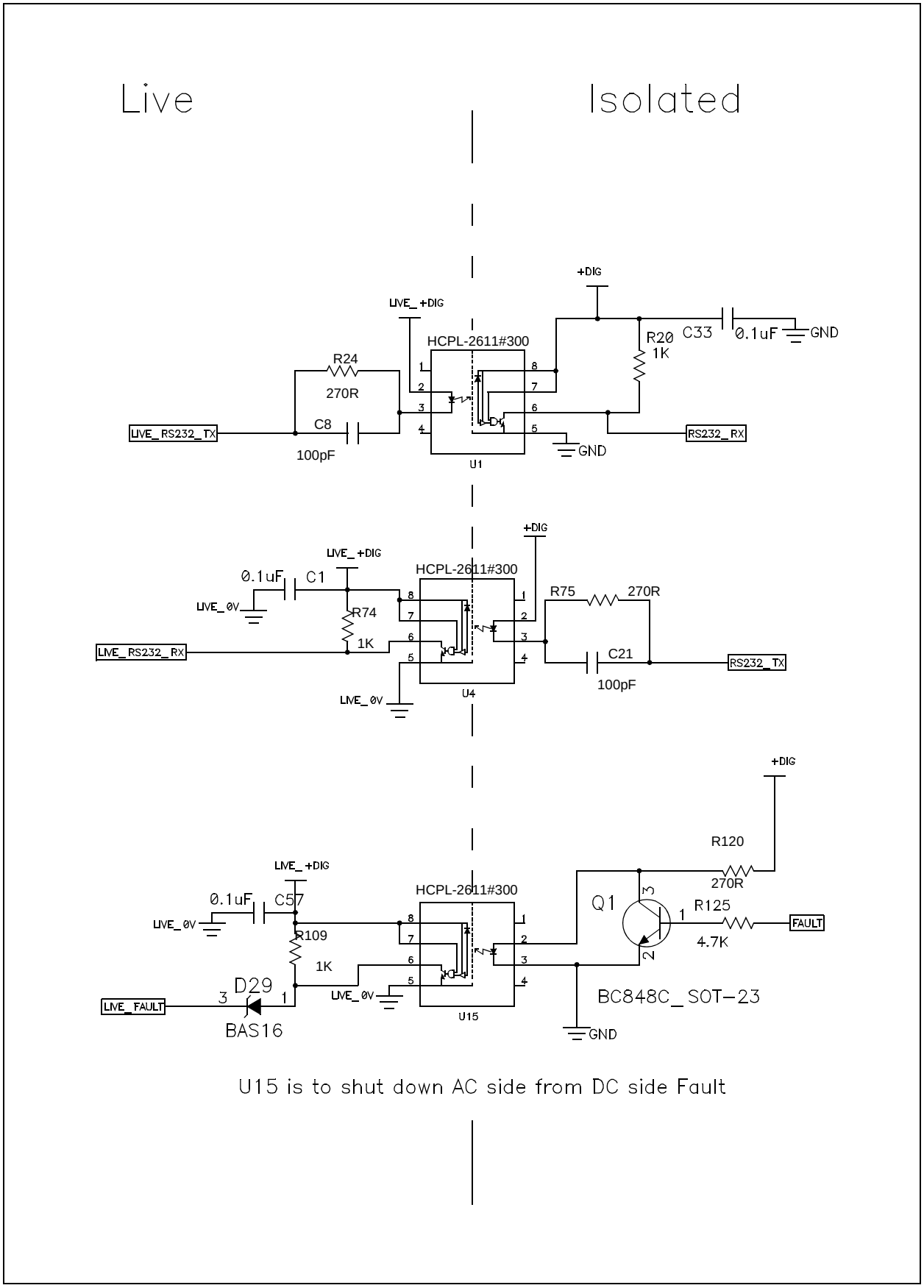


FIGURE A-13: PRIMARY SIDE FEEDBACK CIRCUITS SCHEMATIC

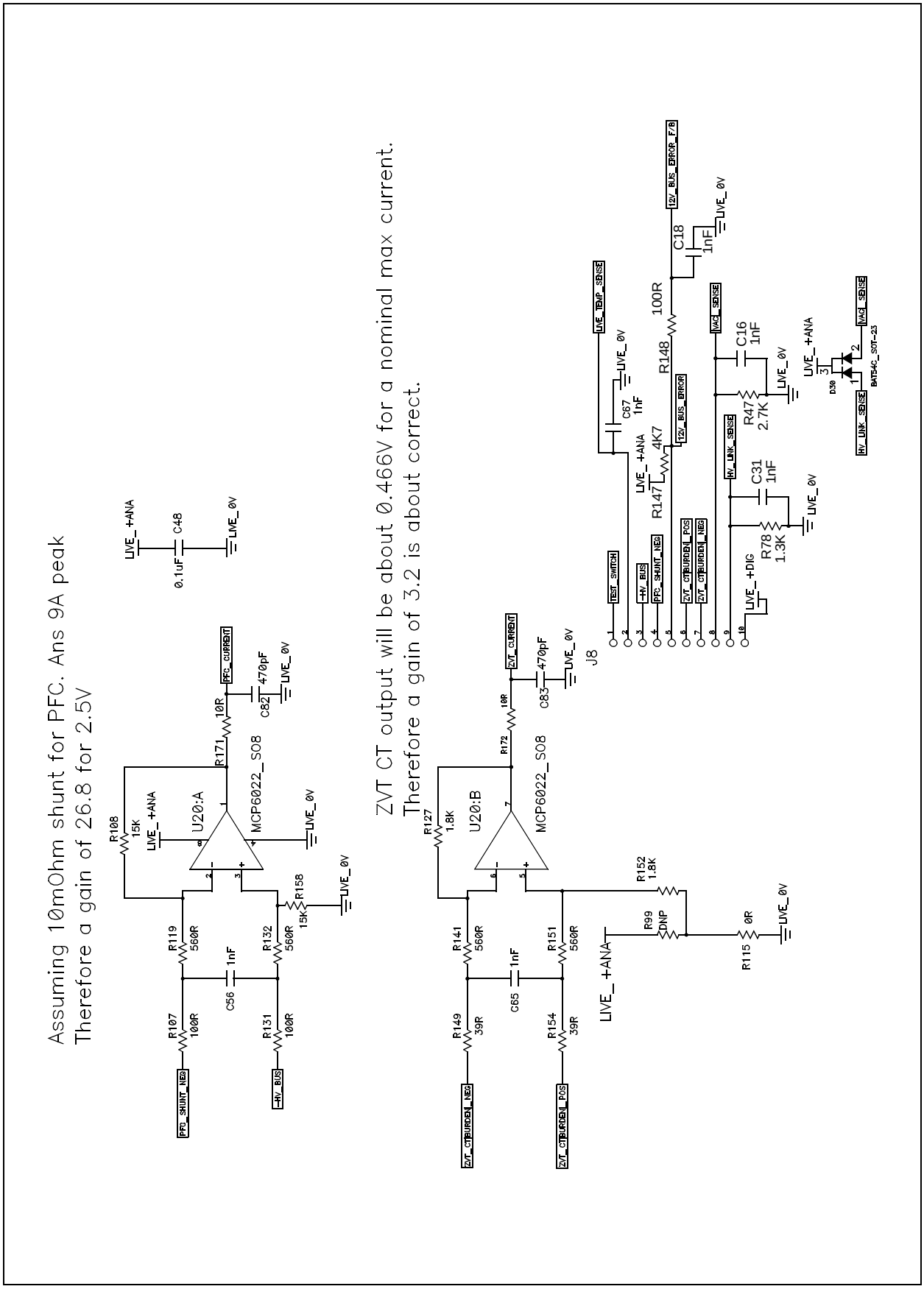


FIGURE A-14: PRIMARY SIDE HARDWARE FAULT CIRCUITRY SCHEMATIC

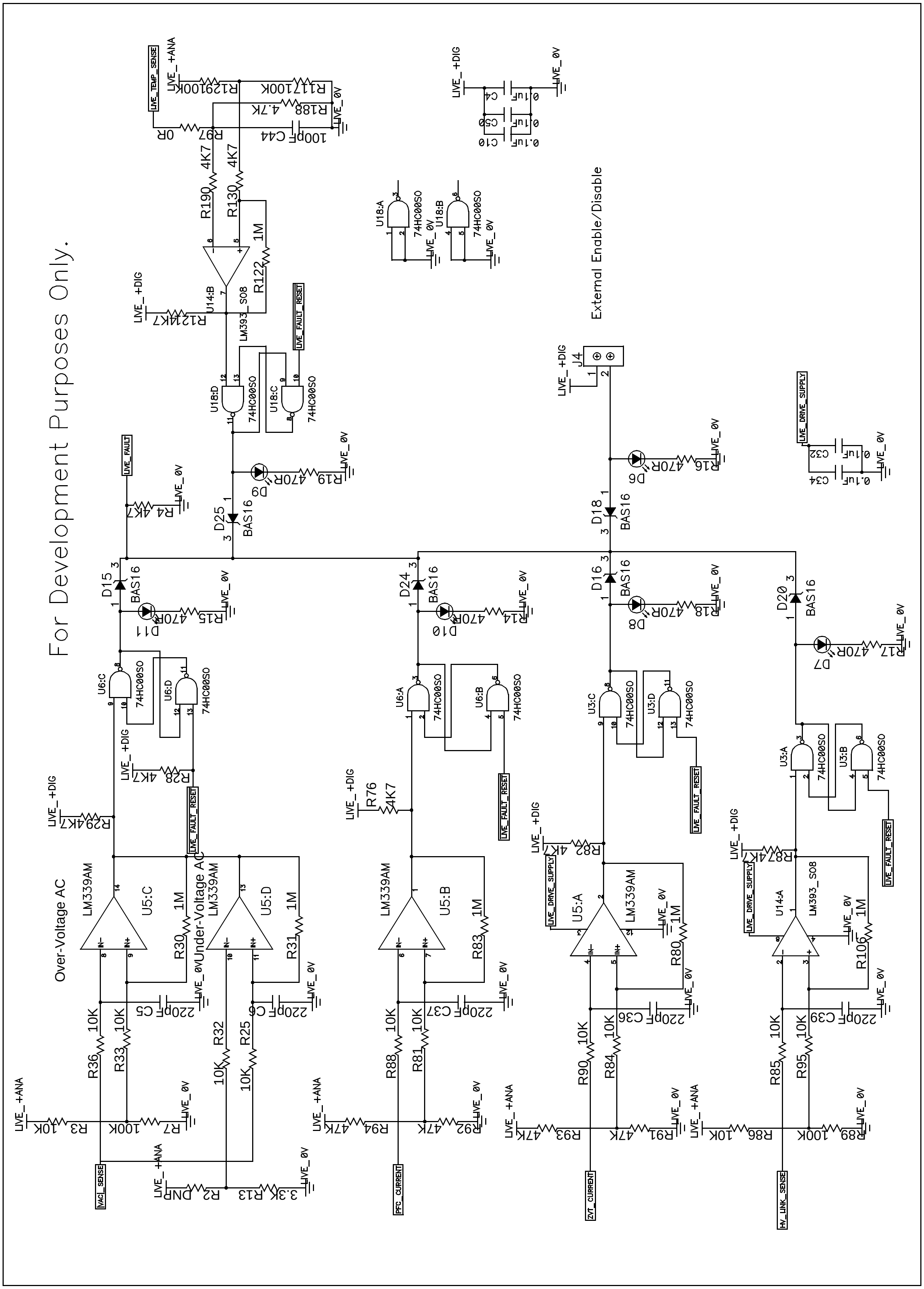


FIGURE A-15: SECONDARY SIDE CONTROLLER SCHEMATIC

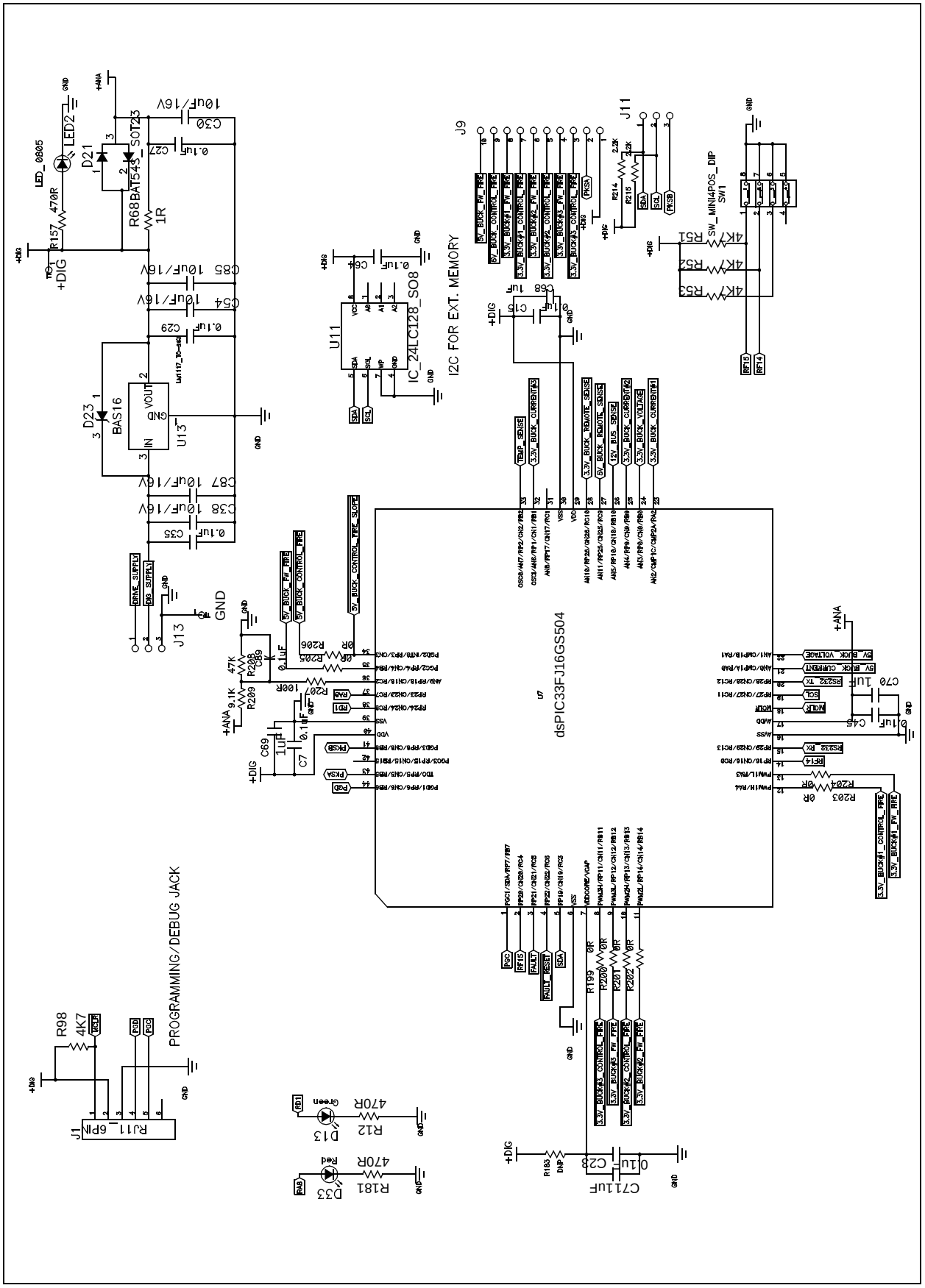


FIGURE A-16: SECONDARY SIDE FEEDBACK SCHEMATIC

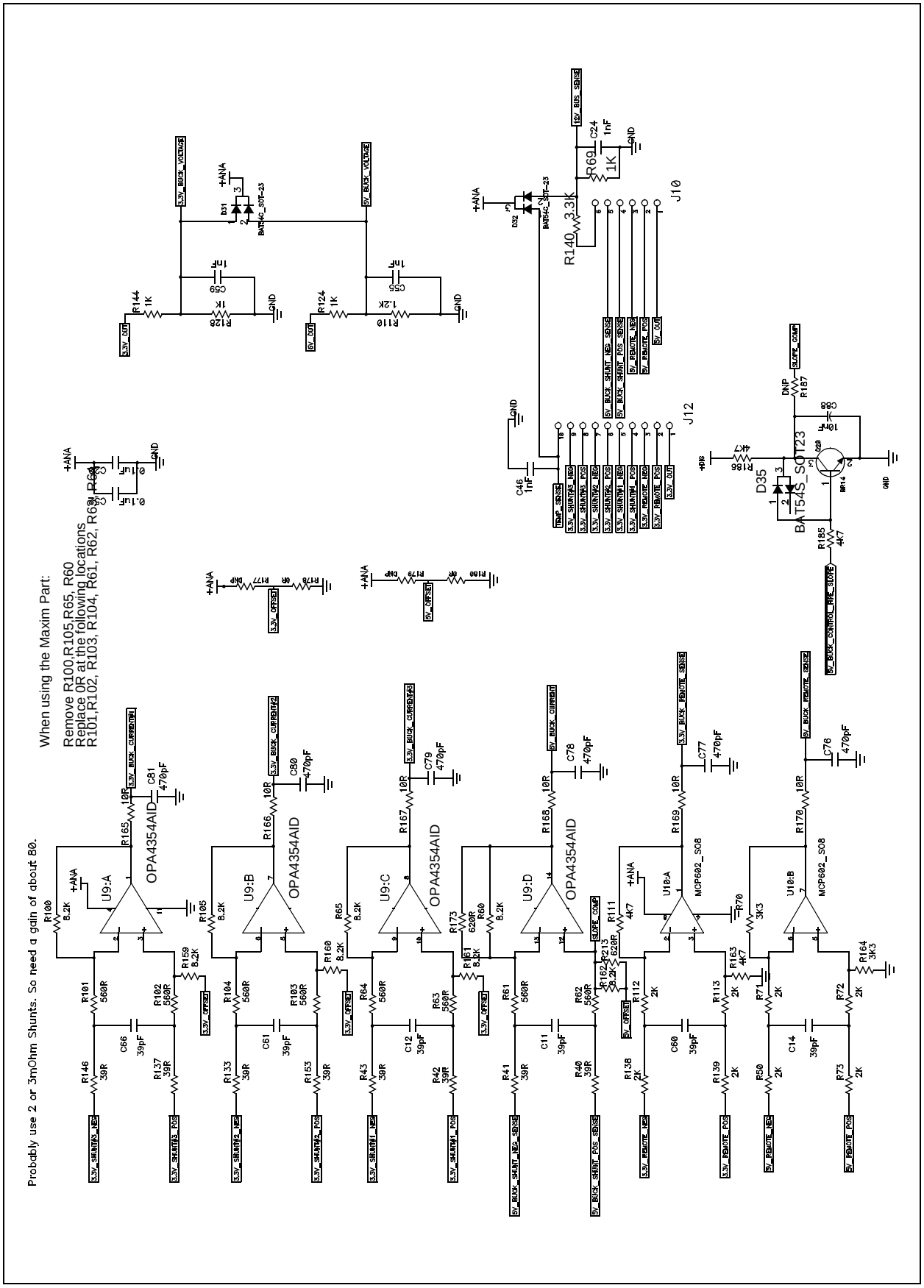
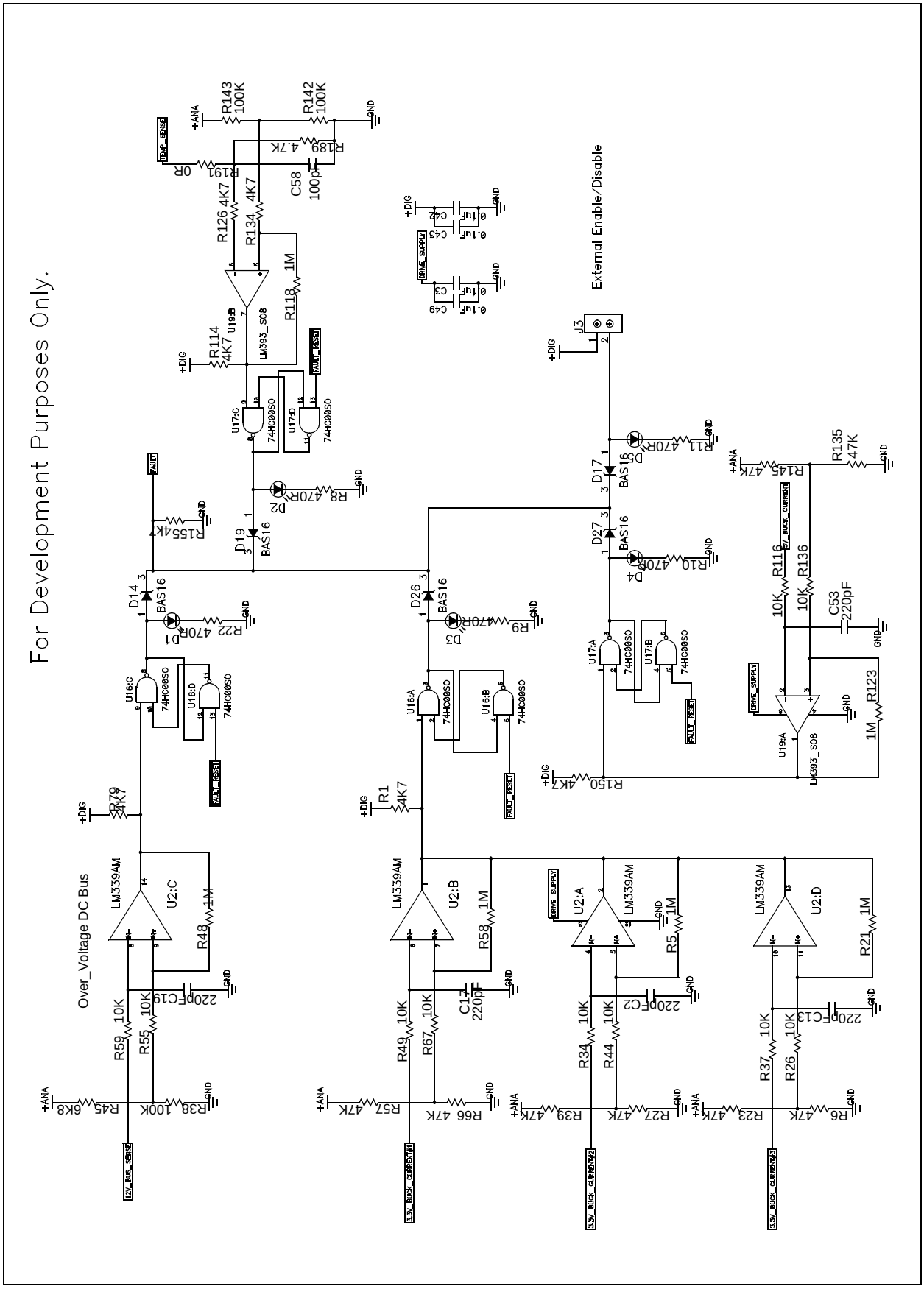


FIGURE A-17: SECONDARY SIDE HARDWARE FAULT CIRCUITS SCHEMATIC



NOTES:

Appendix B. Test Results

This appendix provides information on the test procedures and results for the SMPS AC/DC Reference Design.

The following equipment was used to test the SMPS AC/DC Reference Design:

- Programmable DC Load (or resistive load)
- Two- or Four-Channel Oscilloscope (100 MHz or higher)
- Current probe and Differential probe
- Programmable AC Source, or Variac, or AC Power Cord
- Power Meter
- True RMS Multimeter

B.1 SOFT-START AND OVERSHOOT

The SMPS AC/DC Reference Design has soft-start routines implemented for the PFC Boost converter, ZVT converter, Single-Phase and Multi-Phase Buck converters. The soft-start routines eliminate in-rush current, eliminates overshoot and provides control of the output voltages during start-up. The soft-start scheme is sequenced as follows:

- The PFC Boost converter ramps to 420V,
- the ZVT converter ramps to 12V,
- the Single-Phase Buck converter ramps to 5V,
- and then the Multi-Phase converter ramps to 3.3V.

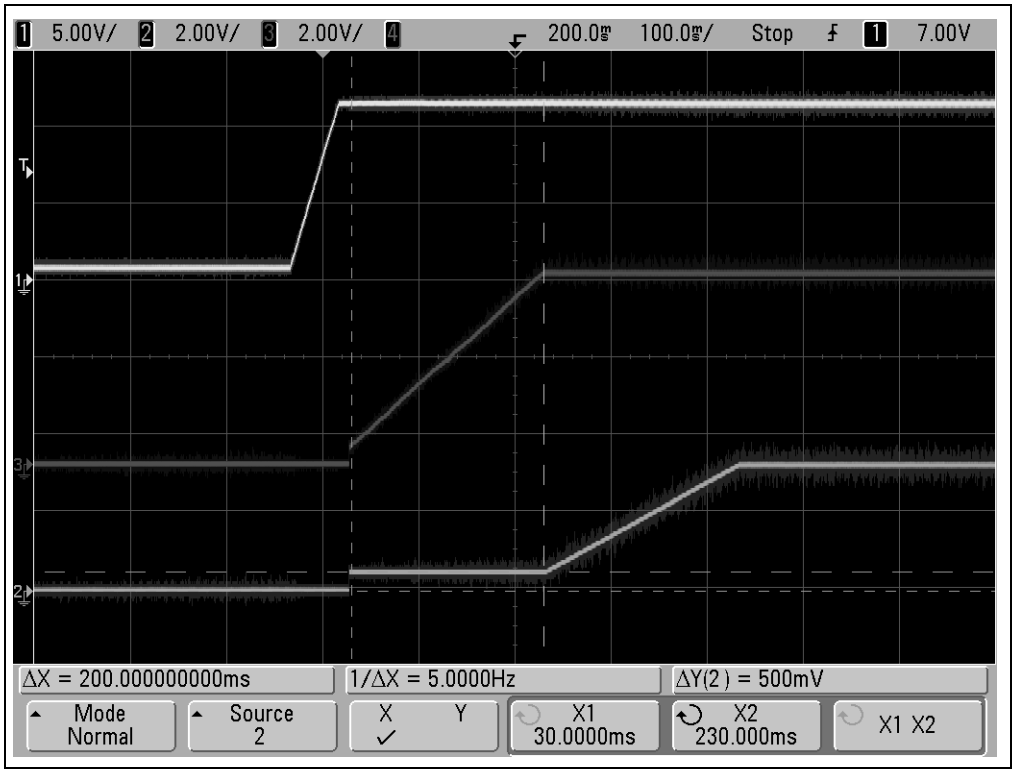
B.1.1 Test Procedure

1. Ensure that the system is off and that all probes are disconnected.
2. Connect the oscilloscope probes across the output terminals (J2, J4, and J17).
3. Set up the oscilloscope for normal trigger mode and on the rising edge of the scope connected to (J2) with a time scale equal to 100 ms or greater. Move the trigger start point to 200 ms.
4. Power on the unit and observe the soft-start.
5. Turn off the system and connect a programmable DC load to any single output or to the 5V and 3.3V outputs simultaneously.
6. Power on the unit and observe the soft-start.
7. Turn off the system and disconnect all probes.

Figure B-1 demonstrates the soft-start sequence for the ZVT converter and the Single-Phase and Multi-Phase converters.

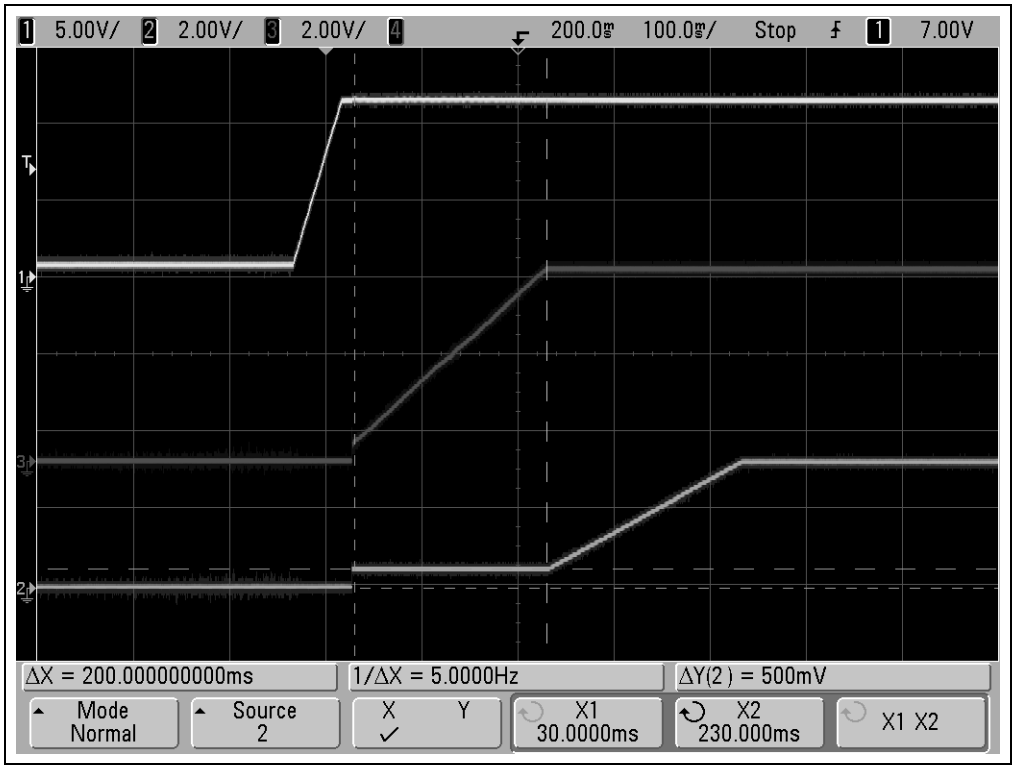
Figure B-2 demonstrates the soft-start sequence with the Single-Phase and Multi-Phase outputs loaded (5V @ 23A, 3.3V @ 35A).

FIGURE B-1: SOFT-START WITHOUT LOAD



Note: The PFC soft-start (not shown in Figure B-1 and Figure B-2) should not be observed simultaneously with the secondary side outputs.

FIGURE B-2: SOFT-START WITH LOAD



B.2 DYNAMIC LOAD RESPONSE

Dynamic load response is measuring the under/overshoot voltage and settling time of the output voltage when performing a load step. The SMPS AC/DC Reference Design has the following load step parameters when the outputs are loaded individually:

- 12V full load step of 30A
- 5V full load step of 23A
- 3.3V full load step of 69A

When the Single-Phase and Multi-Phase converters are loaded simultaneously, the following are the max load steps:

- 5V full load step of 23A
- 3.3V full load step of 56A

The load response of each unit is tested with the following load steps with a maximum slew rate of 1A/us:

- 0-15A and 15-0A (for the 12V output)
- 0-35A and 35-0A (for the 3.3V output)
- 0-12A and 12-0A (for the 5V output)

B.2.1 Test Procedure

1. Ensure that the system is off and that all probes are disconnected.
2. Connect a programmable DC load to any one of the three outputs.
3. Connect the oscilloscope probe across the output terminals with the DC load.
4. Connect the current probe to one of the load cables making sure of the direction of current flow.
5. Set up the oscilloscope for a single capture and trigger on the current probe on either edge and set the oscilloscope channel for AC coupling.
6. Perform the load steps and measure the settling time and under/overshoot voltage.
7. Turn off the system and disconnect all probes.

Figure B-3 through Figure B-8 show the dynamic load response and settling time with 50% load steps.

FIGURE B-3: 12V LOAD RESPONSE 0-15A

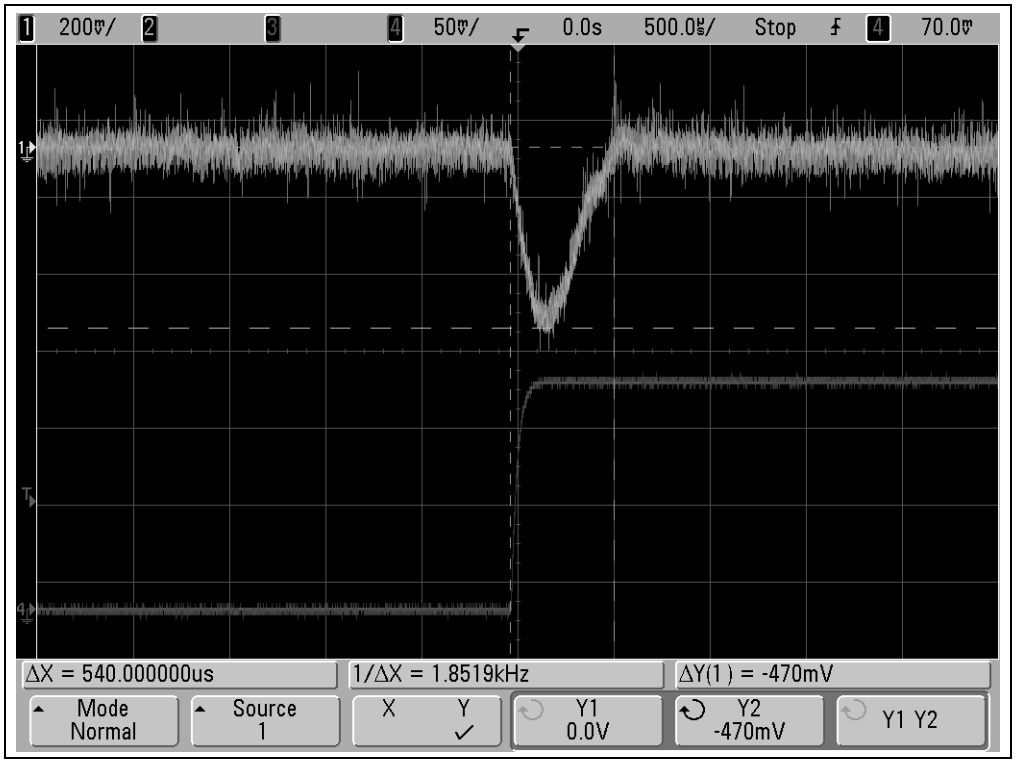


FIGURE B-4: 12V LOAD RESPONSE 15-0A

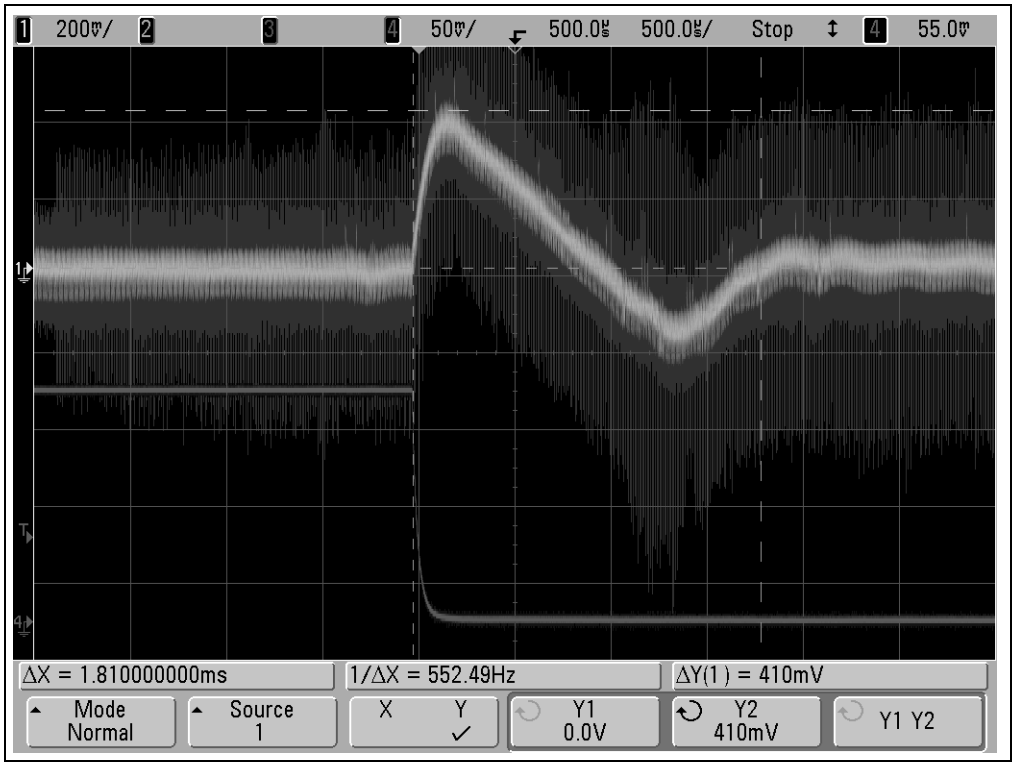


FIGURE B-5: 3.3V LOAD RESPONSE 0-35A

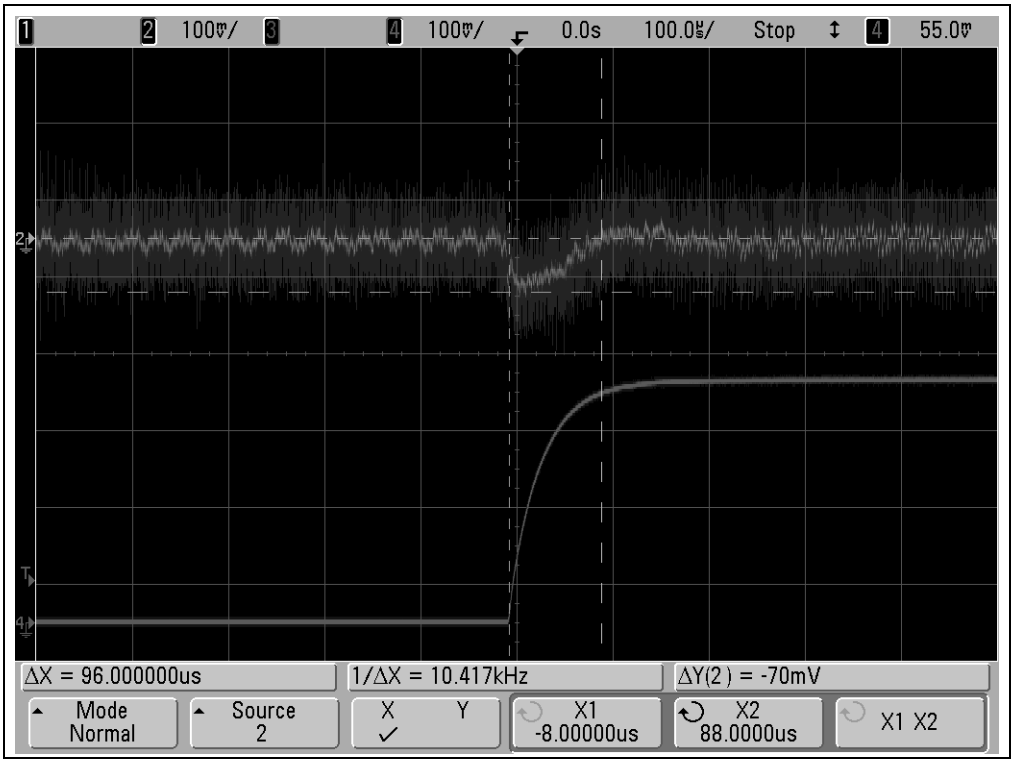


FIGURE B-6: 3.3V LOAD RESPONSE 35-0A

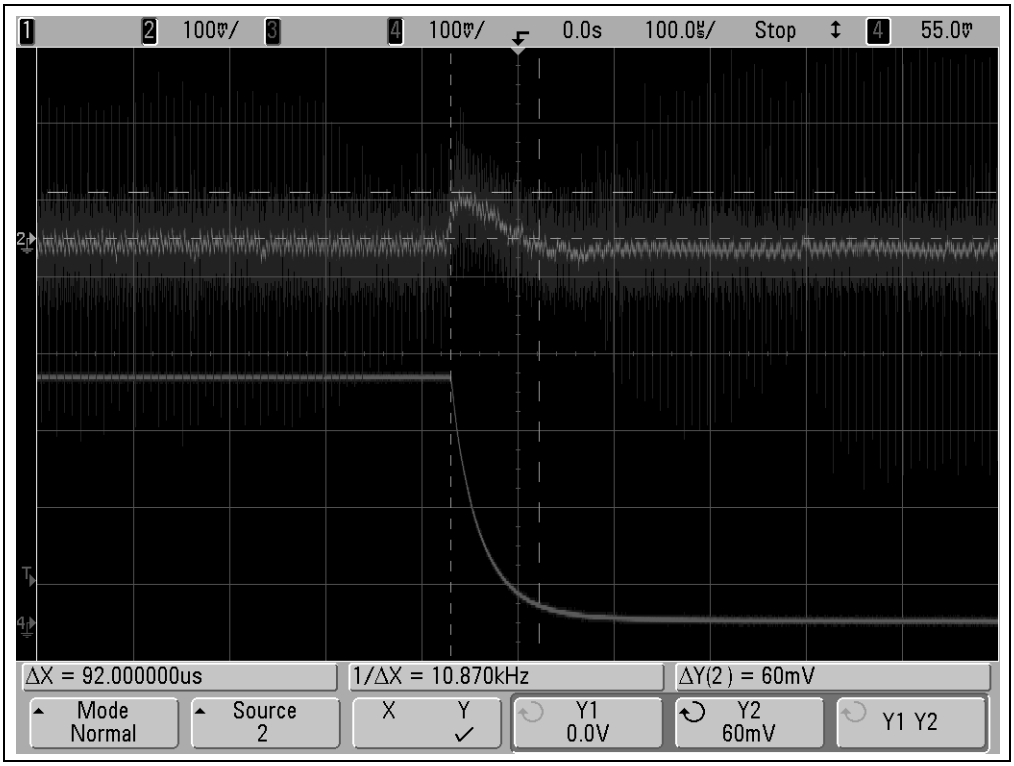


FIGURE B-7: 5V LOAD RESPONSE 0-12A

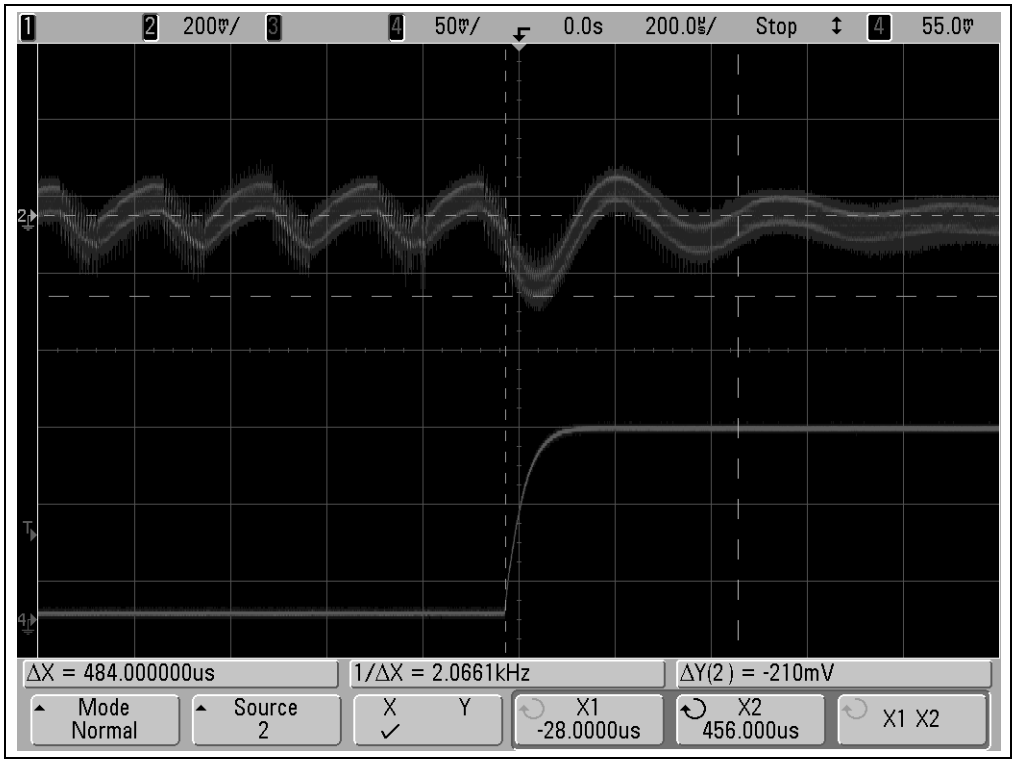
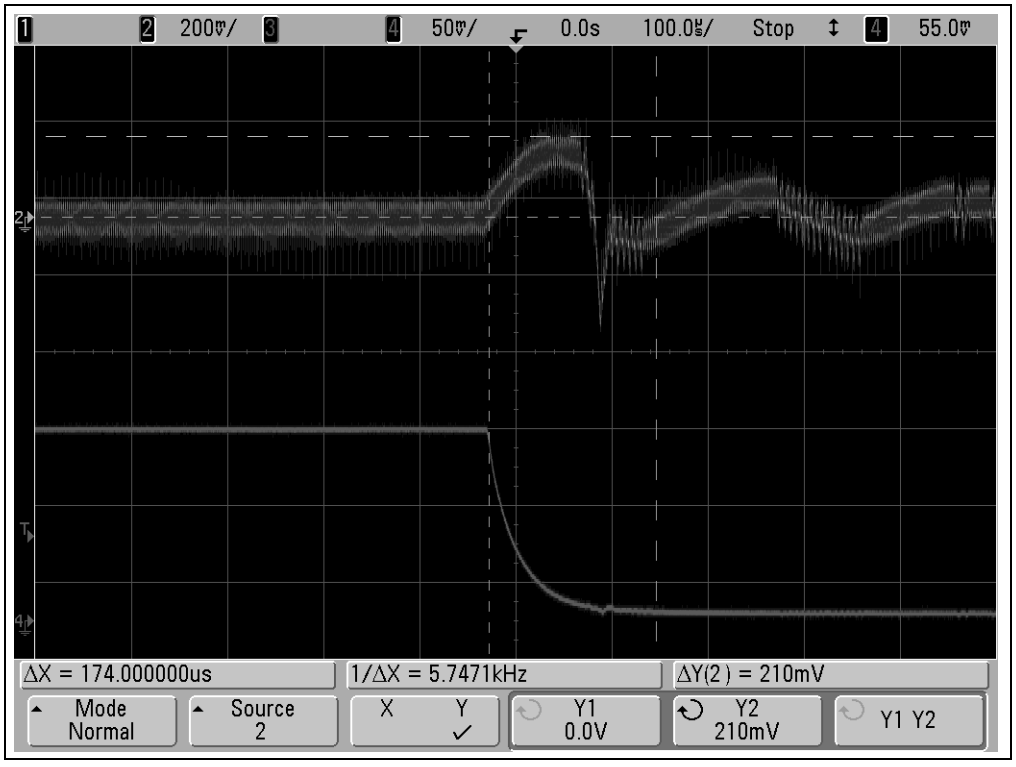


FIGURE B-8: 5V LOAD RESPONSE 12-0A



B.3 OUTPUT VOLTAGE RIPPLE

Output voltage ripple is measured across the output capacitors with the shortest probe ground possible. For production tests, the output voltage ripple is measured at the terminal blocks. Refer to Figure B-9 for the oscilloscope probe connection location used to measure the output voltage ripple.

FIGURE B-9: EXAMPLE OF OSCILLOSCOPE PROBE CONNECTION

B.3.1 Test Procedure

1. Ensure that the system is OFF and all probes are disconnected.
2. Connect the oscilloscope probe across the output capacitor to be measured as shown in Figure B-9.

Note:	Oscilloscope probes should have the shortest ground wire possible to eliminate noise when measuring the ripple voltage.

3. Set up the oscilloscope with a time scale of 2 µs and set the oscilloscope channel to AC coupling and 50 mV per division.
4. Measure the peak-to-peak voltage.
5. To test the output voltage ripple with a load, connect a programmable DC load to the output terminal and re-measure the voltage ripple.
6. Turn off the system and disconnect all probes.

Figure B-10 through Figure B-12 show the output voltage ripple of each stage without load.

FIGURE B-10: 3.3V OUTPUT VOLTAGE RIPPLE

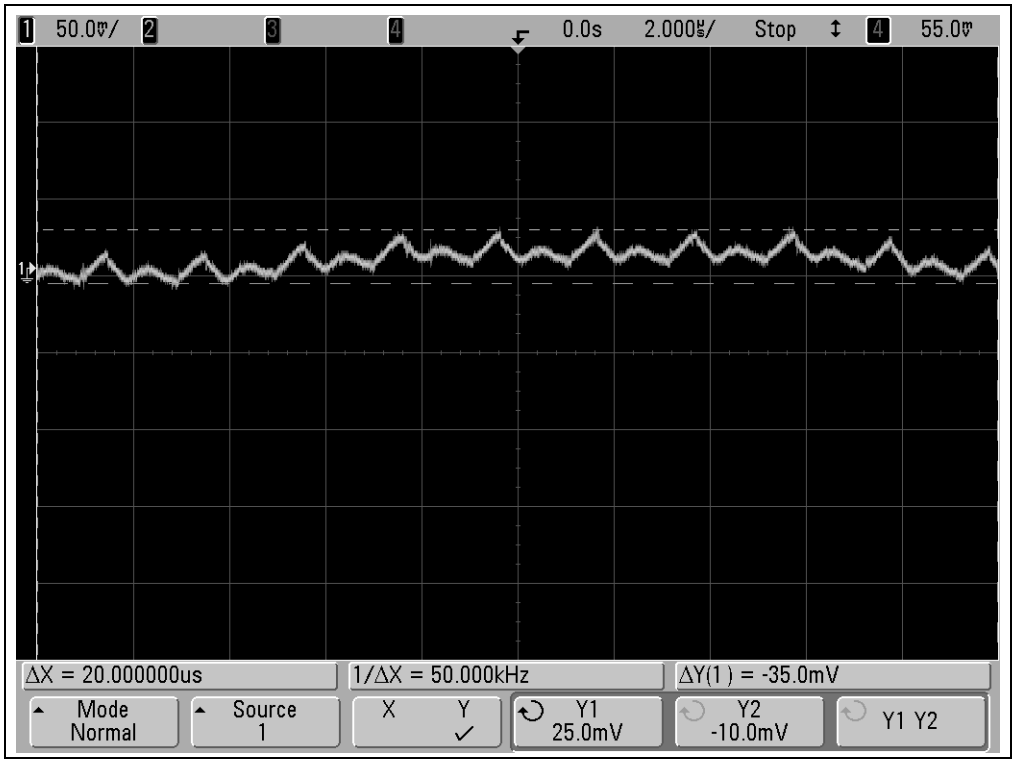


FIGURE B-11: 5V OUTPUT VOLTAGE RIPPLE

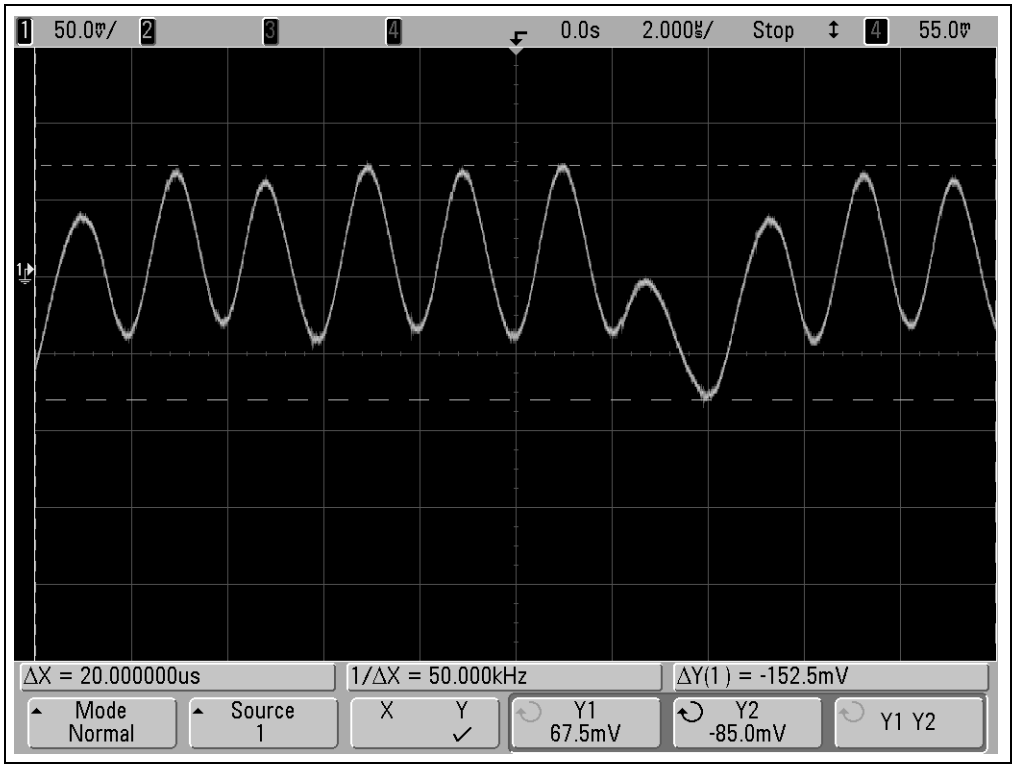
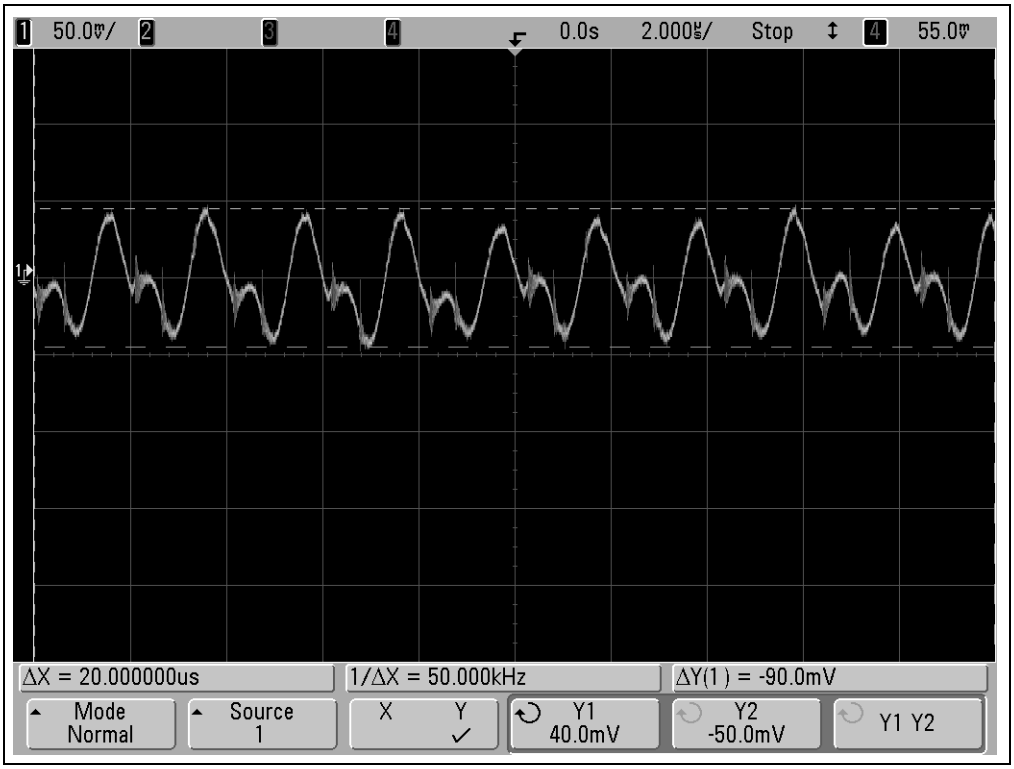


FIGURE B-12: 12V OUTPUT VOLTAGE RIPPLE



B.4 INPUT CURRENT

The SMPS AC/DC Reference Design implements Power Factor Correction (PFC) where the current is in phase with the input voltage.

B.4.1 Test Procedure:

1. Ensure that the system is off and that all probes are disconnected.
2. Connect a differential probe across the input terminal (J16). Connect across the “neutral” and “live” terminals.

WARNING

Do not connect a standard probe across the AC terminal. A differential probe must be used. Failure to heed this warning may result in bodily harm and damage to the oscilloscope and/or SMPS AC/DC Reference Design.

3. Connect the current probe around the live or neutral power cable making sure of the direction of current flow.
4. Set the current probe for 100 mV per Amp and set the oscilloscope channel to a 1:1 ratio.
5. Connect load cables to the 12V output (J1).
6. Verify your connections and turn on the system. You should be able to observe sinusoidal input voltage and current. If not, connect the current probe to the other input.
7. Apply a load to the output and verify that the current and the voltage are still sinusoidal and in phase.
8. Turn off the system and disconnect all probes.

Figure B-13 and Figure B-14 demonstrate the input current and the input voltage at full load operations at 110 VAC and 220 VAC.

FIGURE B-13: INPUT CURRENT AND INPUT VOLTAGE @110 VAC WITH FULL LOAD

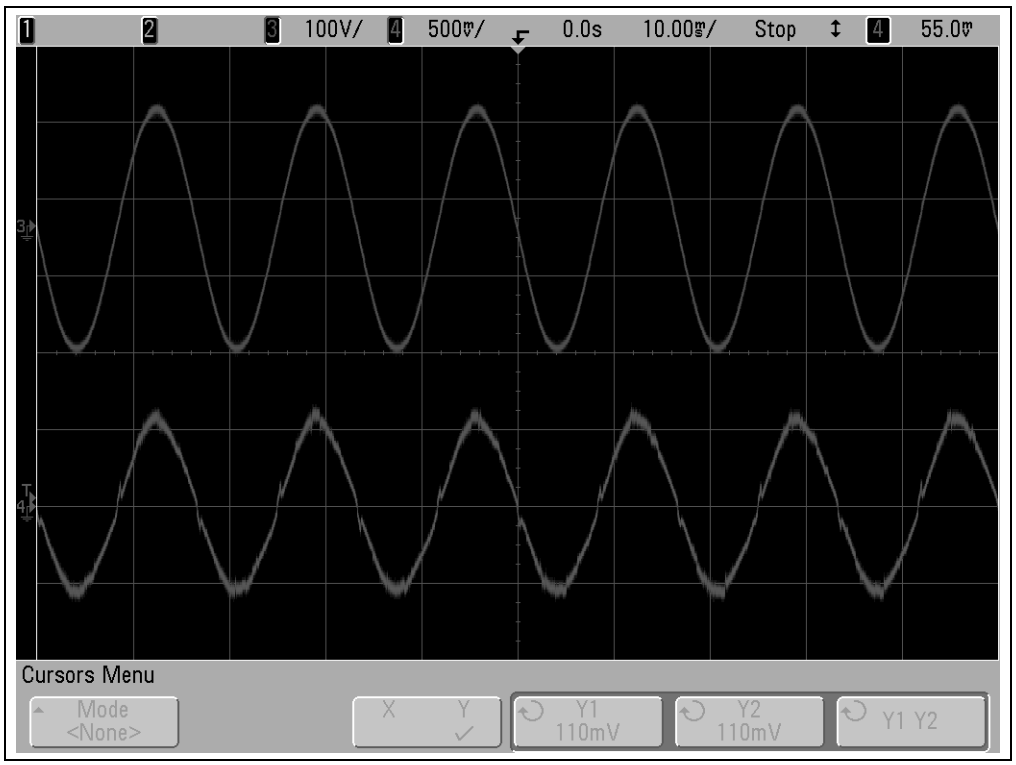
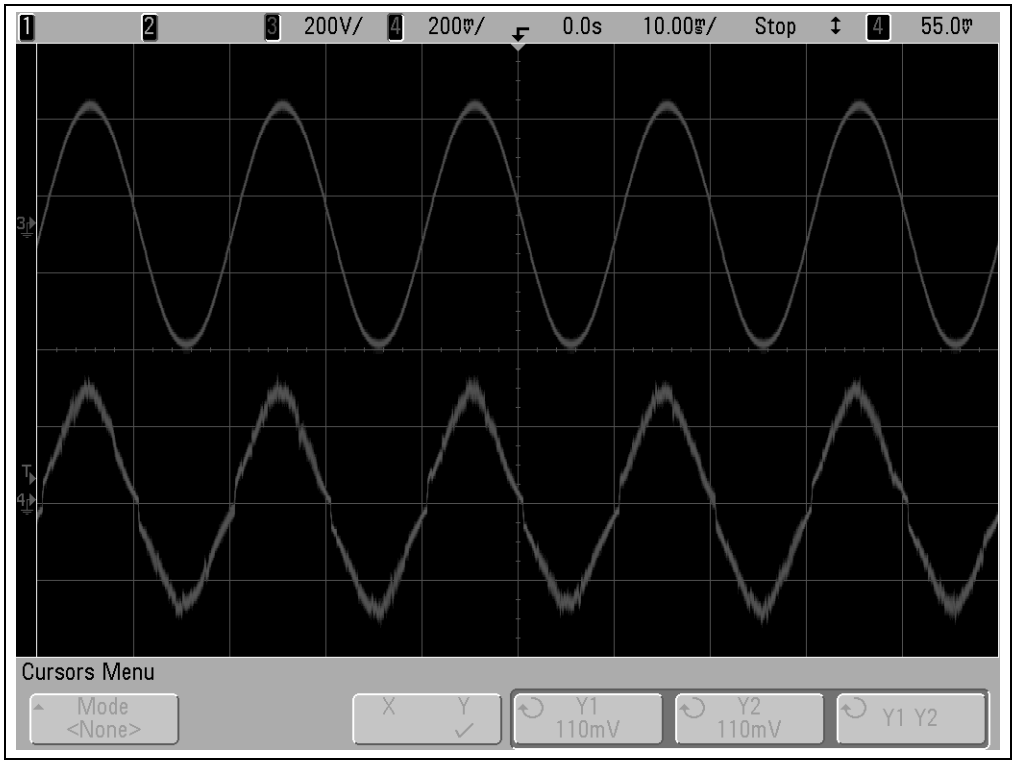


FIGURE B-14: INPUT CURRENT AND INPUT VOLTAGE @ 220 VAC WITH FULL LOAD



B.5 EFFICIENCY

When loading the 12V output ($V_{OUT}1$), the efficiency is approximately 82 percent. If loading the 3.3V and 5V outputs ($V_{OUT}2$ and $V_{OUT}3$) simultaneously, the efficiency is approximately 74 percent at 300W output. Efficiency is measured by dividing the output power by the input power. The power is calculated by multiplying the current (load) by the output voltage. For example, full load on 12V output will yield 360 Watts (12V * 30A = 360W).

If using an AC power cable, connect a true RMS multimeter in series with the power cable to measure the RMS input current, and connect another multimeter in parallel with the power cable to measure RMS input voltage. To calculate input power, multiply the input RMS current by the input RMS voltage. To calculate the percent efficiency divide the output power by the input power and multiply the result by 100.

EXAMPLE B-1:

$I_{OUT}1$ = 0A @ 12V
$I_{OUT}2$ = 56A @ 3.3V
$I_{OUT}3$ = 23A @ 5V

V_{IN} = 110V
I_{IN} = 3.7A

P_{OUT} = ($V_{OUT}1$ * $I_{OUT}1$) + ($V_{OUT}2$ * $I_{OUT}2$) + ($V_{OUT}3$ * $I_{OUT}3$)
= (56A * 3.3V) + (23A * 5V)
= 299.8W

P_{IN} = V_{IN} * I_{IN}
= 407W

Efficiency (%) = P_{OUT} / P_{IN}
= (299.8 / 407) * 100
= 73.7%

B.6 INPUT CURRENT TOTAL HARMONIC DISTORTION (ITHD)

Using a Voltech PM100 or similar power meter, measure the ITHD. ITHD is tested at the following conditions:

- V_{IN} = 110V @ 60 Hz @ Full Load
- V_{IN} = 220V @ 50 Hz @ Full Load

The current ITHD measurements of the SMPS AC/DC Reference Design at 110 V_{AC} is approximately 4.8% and the ITHD at 220 V_{AC} is approximately 6%.

B.7 POWER FACTOR

Using a Voltech PM100 or similar power meter, measure the power factor. The power factor of each reference design is tested at the following:

- V_{IN} = 110V @ 60 Hz @ Full Load
- V_{IN} = 220V @ 50 Hz @ Full Load
- V_{IN} = 110V @ 60 Hz @ No Load
- V_{IN} = 220V @ 50 Hz @ No Load

The current power factor of the SMPS AC/DC Reference Design at 110V at full load is .998 and the power factor at 220V at full load is .99.

B.8 TEST RESULTS TABLE

Each SMPS AC/DC Reference Design is extensively tested from no/full load starts to maximum current steps across the universal input voltage range. In addition, each unit passes a rigorous 12-hour burn-in test at full load (300W). The following table shows the complete list of tests performed on the SMPS AC/DC Reference Design before the unit is shipped.

TABLE B-1: TEST RESULTS TABLE

Tests	Min	Max	Units	Result	Remarks
Input Current					
Max input current at 110 VAC	—	5	A	3.75	Loading VOUT2 @ 56A and VOUT3 @ 23A
Max input current at 220 VAC	—	1.8	A	1.73	Loading VOUT2 @ 56A and VOUT3 @ 23A
Maximum in-rush current at VIN @ 220 VAC @ No Load	—	35	A	27	
Output Overshoot at Start-up					
VIN = 110 VAC					
VOUT1 @ 0A	—	12.48	V	12	
VOUT2 @ 0A	—	3.432	V	3.3	
VOUT3 @ 0A	—	5.2	V	5	
VIN = 220 VAC					
VOUT1 @ 0A	—	12.48	V	12	
VOUT2 @ 0A	—	3.432	V	3.3	
VOUT3 @ 0A	—	5.2	V	5	
Power Factor					
VIN = 110 VAC @ No Load @ 60Hz	0.9	—	—	0.974	
VIN = 220 VAC @ No Load @ 50Hz	0.8	—	—	0.855	
VIN = 110 VAC @ Full Load @ 60Hz	0.98	—	—	0.997	
VIN = 220 VAC @ Full Load @ 50Hz	0.97	—	—	0.989	
Input current THD @ VTHD @ 2%					Measured by power meter
VIN = 110 VAC @ Full Load @ 60Hz	—	5	%	4.9	
VIN = 220 VAC @ Full Load @ 50Hz	—	7	%	6	
Input Power					
VOUT1 @ 30 A, VIN @ 110 VAC	—	—	watt	445	
VOUT1 @ 0A, VOUT2 @ 56A, VOUT3 @ 23A, VIN @ 110 VAC	—	—	watt	415	
VOUT1 @ 30 A, VIN @ 220 VAC	—	—	watt	431	
VOUT1 @ 0A, VOUT2 @ 56A, VOUT3 @ 23A, VIN @ 220 VAC	—	—	watt	400	

TABLE B-1: TEST RESULTS TABLE (CONTINUED)

Tests	Min	Max	Units	Result	Remarks
Set Point Voltage (@ 110 VAC)					
Set point voltage of 12V (VOUT1) @ 15A	11.94	12.06	Volt	11.97	
Set point voltage of 3.3V (VOUT2) @ 35A	3.2835	3.3165	Volt	3.31	
Set point voltage of 5V (VOUT3) @ 12A	4.98	5.02	Volt	4.98	
Line & Load Regulation					Measure output voltage with multimeter
VIN = 110 VAC					
VOUT1 @ 0A	11.94	12.06	Volt	11.98	
VOUT1 @ 30A	11.88	12.12	Volt	11.97	
VOUT2 @ 0A	3.2835	3.3165	Volt	3.32	
VOUT2 @ 69A	3.2835	3.3165	Volt	3.3	
VOUT3 @ 0A	4.98	5.02	Volt	5.01	
VOUT3 @ 23A	4.98	5.02	Volt	4.98	
VIN = 220 VAC					
VOUT1 @ 0A	11.94	12.06	Volt	11.98	
VOUT1 @ 30A	11.88	12.12	Volt	11.96	
VOUT2 @ 0A	3.2835	3.3165	Volt	3.32	
VOUT2 @ 69A	3.2835	3.3165	Volt	3.3	
VOUT3 @ 0A	4.98	5.02	Volt	5.01	
VOUT3 @ 23A	4.98	5.02	Volt	4.98	
Output Voltage Ripple					
VIN = 110 VAC					
VOUT1 @ 0A	—	—	mV	130	Measured at output terminals(1)
VOUT1 @ 30A	—	—	mV	160	Measured at output terminals(1)
VOUT2 @ 0A	—	—	mV	90	Measured at output terminals(1)
VOUT2 @ 69A	—	—	mV	90	Measured at output terminals(1)
VOUT3 @ 0A	—	—	mV	160	Measured at output terminals(1)
VOUT3 @ 23A	—	—	mV	130	Measured at output terminals(1)
Dynamic Load Response Slew Rate = 1A/µs (Tests @ 110 VAC)					
VOUT2 = 0A, VOUT3 = 0A, VOUT1 = 0A-15A	—	—	mV	470	
VOUT2 = 0A, VOUT3 = 0A, VOUT1 = 15A-0A	—	—	mV	380	
VOUT1 = 0A, VOUT3 = 0A, VOUT2 = 0A-35A	—	—	mV	100	
VOUT1 = 0A, VOUT3 = 0A, VOUT2 = 35A-0A	—	—	mV	100	
VOUT1= 0A, VOUT2 = 0A, VOUT3 = 0A-12A	—	—	mV	190	
VOUT1= 0A, VOUT2 = 0A, VOUT3 = 12A-0A	—	—	mV	210	

Note 1: See **Section B.3 "Output Voltage Ripple"** for details on how to measure output voltage ripple.

TABLE B-1: TEST RESULTS TABLE (CONTINUED)

Tests	Min	Max	Units	Result	Remarks
Settle Time (@ 110 VAC)					
VOUT2 = 0A, VOUT3 = 0A, VOUT1 = 0A-15A	—	—	us	656	
VOUT2 = 0A, VOUT3 = 0A, VOUT1 = 15A-0A	—	—	us	1976	
VOUT1 = 0A, VOUT3 = 0A, VOUT2 = 0A-35A	—	—	us	120	
VOUT1 = 0A, VOUT3 = 0A, VOUT2 = 35A-0A	—	—	us	88	
VOUT1= 0A, VOUT2 = 0A, VOUT3 = 0A-12A	—	—	us	528	
VOUT1= 0A, VOUT2 = 0A, VOUT3 = 12A-0A	—	—	us	225	
Efficiency @ 110 VAC					
Efficiency when 12 @30A	—	—	%	81	
Efficiency when 3.3V@56A and 5V@23A	—	—	%	72	
Set Point Limits					
Input Under Voltage Lock-out (no load)	75	—	VAC	76.3	
Input Over Voltage Lock-out (no load)	—	270	VAC	269	
5V over-current limit	—	27	A	25.4	
3.3V over-current limit	—	75	A	74	
Full Load Start (Pass or Fail)					
VOUT1= 0A, VOUT2 = 56A, VOUT3 = 23A @ 85 VAC	—	—	—	Pass	
VOUT1= 0A, VOUT2 = 56A, VOUT3 = 23A @ 110 VAC	—	—	—	Pass	
VOUT1= 0A, VOUT2 = 56A, VOUT3 = 23A @ 220 VAC	—	—	—	Pass	
VOUT1= 0A, VOUT2 = 56A, VOUT3 = 23A @ 265 VAC	—	—	—	Pass	
VOUT1= 0A, VOUT2 = 69A, VOUT3 = 0A @ 85 VAC	—	—	—	Pass	
VOUT1= 0A, VOUT2 = 69A, VOUT3 = 0A @ 110 VAC	—	—	—	Pass	
VOUT1= 0A, VOUT2 = 69A, VOUT3 = 0A @ 220 VAC	—	—	—	Pass	
VOUT1= 0A, VOUT2 = 69A, VOUT3 = 0A @ 265 VAC	—	—	—	Pass	
VOUT1= 30A, VOUT2 = 0A, VOUT3 = 0A @ 85 VAC	—	—	—	Pass	
VOUT1= 30A, VOUT2 = 0A, VOUT3 = 0A @ 110 VAC	—	—	—	Pass	
VOUT1= 30A, VOUT2 = 0A, VOUT3 = 0A @ 220 VAC	—	—	—	Pass	
VOUT1= 30A, VOUT2 = 0A, VOUT3 = 0A @ 265 VAC	—	—	—	Pass	
No Load Start					
VOUT1= 0A, VOUT2 = 0A, VOUT3 = 0A @ 85 VAC	—	—	—	Pass	
VOUT1= 0A, VOUT2 = 0A, VOUT3 = 0A @ 110 VAC	—	—	—	Pass	
VOUT1= 0A, VOUT2 = 0A, VOUT3 = 0A @ 220 VAC	—	—	—	Pass	
VOUT1= 0A, VOUT2 = 0A, VOUT3 = 0A @ 265 VAC	—	—	—	Pass	

TABLE B-1: TEST RESULTS TABLE (CONTINUED)

Tests	Min	Max	Units	Result	Remarks
Max Current Steps					Pass or Fail (If Fail, what is max current step)
VOUT1 (0-30A, 30-0A) @ 85 VAC	—	—	—	Pass	
VOUT1 (0-30A, 30-0A) @ 110 VAC	—	—	—	Pass	
VOUT1 (0-30A, 30-0A) @ 220 VAC	—	—	—	Pass	
VOUT1 (0-30A, 30-0A) @ 265 VAC	—	—	—	Pass	
					Not measured with time (12-hour burn-in is done @ 56A)
VOUT2 (0-69A, 69-0A) @ 85 VAC	—	—	—	Pass	
VOUT2 (0-69A, 69-0A) @ 110 VAC	—	—	—	Pass	
VOUT2 (0-69A, 69-0A) @ 220 VAC	—	—	—	Pass	
VOUT2 (0-69A, 69-0A) @ 265 VAC	—	—	—	Pass	
VOUT3 (0-23A, 23-0A) @ 85 VAC	—	—	—	Pass	
VOUT3 (0-23A, 23-0A) @ 110 VAC	—	—	—	Pass	
VOUT3 (0-23A, 23-0A) @ 220 VAC	—	—	—	Pass	
VOUT3 (0-23A, 23-0A) @ 265 VAC	—	—	—	Pass	
					Full Load steps with VOUT2 while VOUT3 loaded
VOUT2 (0-56A, 56-0A) VOUT3 @ 23A @ 85 VAC	—	—	—	Pass	
VOUT2 (0-56A, 56-0A) VOUT3 @ 23A @ 110 VAC	—	—	—	Pass	
VOUT2 (0-56A, 56-0A) VOUT3 @ 23A @ 220 VAC	—	—	—	Pass	
VOUT2 (0-56A, 56-0A) VOUT3 @ 23A @ 265 VAC	—	—	—	Pass	
					Full Load steps with VOUT3 while VOUT2 loaded
VOUT2 @ 56A, VOUT3 (0-23A, 23-0A) @ 85 VAC	—	—	—	Pass	
VOUT2 @ 56A, VOUT3 (0-23A, 23-0A) @ 110 VAC	—	—	—	Pass	
VOUT2 @ 56A, VOUT3 (0-23A, 23-0A) @ 220 VAC	—	—	—	Pass	
VOUT2 @ 56A, VOUT3 (0-23A, 23-0A) @ 265 VAC	—	—	—	Pass	

Burn-in Test for 12Hrs continuous @ 300W, VOUT2 @ 56A, VOUT3 @ 23A					
VOUT1	11.94	12.06	Volt	Pass	Measured 11.95
VOUT2	3.2835	3.3165	Volt	Pass	Measured 3.3
VOUT3	4.98	5.02	Volt	Pass	Measured 4.98

Extended Temperature Tests @ 225W, 50° C		
VOUT2 @ 42A, VOUT3 @ 17A	Pass	Not characterized on all units

NOTES:

Appendix C. References

This section provides the list of references used throughout this document.

[1]Herfurth, M., *"Active Harmonic Filtering for Line Rectifiers of Higher Output Power"*, Siemens Components XXI (1986), No. 1, pp. 9 - 13.

[2]Zhou, C.and Jovanovic, M.M., *"Design Trade-offs in Continuous Current-Mode Controlled Boost Power-Factor Correction Circuits"*, Proceedings of HFPC '92, May 1992, pp. 209 - 219.

[3]Chen, W, Lee, F. C., Jovanovic, M. M., and Sabate, J. A., *"A Comparative Study of a Class of Full Bridge Zero-Voltage-Switched PWM Converters"*, Proceedings of APEC '95, pp. 893 - 899.

[4]Frank, W., Dahlquist, F., Kapels, H., Schmitt, M., and Deboy, G., *"Compensation MOSFETs with Fast Body Diode - Benefits in Performance and Reliability in ZVS Applications"*. Proceedings of IPECSA, the International Power Electronics Component Systems Applications Conference, San Francisco, CA, USA, March 29 - April 1, 2004.

[5]Snelling, E.C., *"Soft Ferrites. Properties and Applications"*, 2nd Edition, Butterworths, London, UK, 1988.

[6]Jongsma, J., *"High-Frequency Ferrite Power Transformer and Choke Design - Part 3 Transformer Winding Design"*, N. V. Philips, September 1982.

[7]Dowell, P. L., "Effects of Eddy Currents in Transformer Windings", Proceedings of the IEE, Vol. 113, No. 8, August 1966, pp. 1387 - 1394.

[8]McLyman, C. W. T., "Transformer and Inductor Design Handbook", 3rd edition, Marcel Dekker Inc., New York, USA, 2004.

[9]*"MOSFETs Move in on Low Voltage Rectification"*, MOSPOWER Applications Handbook, Siliconix, 1984, pp. 5-69 - 5-86.

[10]Kutkut, N. H., Divan, D. M., and Gascoigne, R. W., *"An Improved Full-Bridge Zero-Voltage-Switching PWM Converter Using a Two-Inductor Rectifier"*, IEEE Transactions on Industry Applications, Vol. 31, No. 1, January/February 1995, pp. 119 - 126

[11]Alivio, G., Ambrus, J., McDonald, T., and Dowling, R., *"Maximizing the Effectiveness of your SMD Assemblies"*, Application Note AN-994, International Rectifier.

[12]Wei, J. and Lee, F. C., *"An Output Impedance-based Design of Voltage Regulator Output Capacitors for High Slew-rate Load Current Transients"*, Proceedings of IEEE APEC 2004, pp. 304 - 310.

[13]*"12 W Input Universal CV Adapter"*, Power Integrations Design Idea DI-91, January 2006.

NOTES:

Index

NOTES:

Worldwide Sales and Service

AMERICAS

Corporate Office
2355 West Chandler Blvd.
Chandler, AZ 85224-6199
Tel: 480-792-7200
Fax: 480-792-7277
Technical Support:
http://support.microchip.com
Web Address:
www.microchip.com

Atlanta
Duluth, GA
Tel: 678-957-9614
Fax: 678-957-1455

Boston
Westborough, MA
Tel: 774-760-0087
Fax: 774-760-0088

Chicago
Itasca, IL
Tel: 630-285-0071
Fax: 630-285-0075

Dallas
Addison, TX
Tel: 972-818-7423
Fax: 972-818-2924

Detroit
Farmington Hills, MI
Tel: 248-538-2250
Fax: 248-538-2260

Kokomo
Kokomo, IN
Tel: 765-864-8360
Fax: 765-864-8387

Los Angeles
Mission Viejo, CA
Tel: 949-462-9523
Fax: 949-462-9608

Santa Clara
Santa Clara, CA
Tel: 408-961-6444
Fax: 408-961-6445

Toronto
Mississauga, Ontario,
Canada
Tel: 905-673-0699
Fax: 905-673-6509

ASIA/PACIFIC

Asia Pacific Office
Suites 3707-14, 37th Floor
Tower 6, The Gateway
Harbour City, Kowloon
Hong Kong
Tel: 852-2401-1200
Fax: 852-2401-3431

Australia - Sydney
Tel: 61-2-9868-6733
Fax: 61-2-9868-6755

China - Beijing
Tel: 86-10-8528-2100
Fax: 86-10-8528-2104

China - Chengdu
Tel: 86-28-8665-5511
Fax: 86-28-8665-7889

China - Hong Kong SAR
Tel: 852-2401-1200
Fax: 852-2401-3431

China - Nanjing
Tel: 86-25-8473-2460
Fax: 86-25-8473-2470

China - Qingdao
Tel: 86-532-8502-7355
Fax: 86-532-8502-7205

China - Shanghai
Tel: 86-21-5407-5533
Fax: 86-21-5407-5066

China - Shenyang
Tel: 86-24-2334-2829
Fax: 86-24-2334-2393

China - Shenzhen
Tel: 86-755-8203-2660
Fax: 86-755-8203-1760

China - Wuhan
Tel: 86-27-5980-5300
Fax: 86-27-5980-5118

China - Xiamen
Tel: 86-592-2388138
Fax: 86-592-2388130

China - Xian
Tel: 86-29-8833-7252
Fax: 86-29-8833-7256

China - Zhuhai
Tel: 86-756-3210040
Fax: 86-756-3210049

ASIA/PACIFIC

India - Bangalore
Tel: 91-80-4182-8400
Fax: 91-80-4182-8422

India - New Delhi
Tel: 91-11-4160-8631
Fax: 91-11-4160-8632

India - Pune
Tel: 91-20-2566-1512
Fax: 91-20-2566-1513

Japan - Yokohama
Tel: 81-45-471- 6166
Fax: 81-45-471-6122

Korea - Daegu
Tel: 82-53-744-4301
Fax: 82-53-744-4302

Korea - Seoul
Tel: 82-2-554-7200
Fax: 82-2-558-5932 or
82-2-558-5934

Malaysia - Kuala Lumpur
Tel: 60-3-6201-9857
Fax: 60-3-6201-9859

Malaysia - Penang
Tel: 60-4-227-8870
Fax: 60-4-227-4068

Philippines - Manila
Tel: 63-2-634-9065
Fax: 63-2-634-9069

Singapore
Tel: 65-6334-8870
Fax: 65-6334-8850

Taiwan - Hsin Chu
Tel: 886-3-572-9526
Fax: 886-3-572-6459

Taiwan - Kaohsiung
Tel: 886-7-536-4818
Fax: 886-7-536-4803

Taiwan - Taipei
Tel: 886-2-2500-6610
Fax: 886-2-2508-0102

Thailand - Bangkok
Tel: 66-2-694-1351
Fax: 66-2-694-1350

EUROPE

Austria - Wels
Tel: 43-7242-2244-39
Fax: 43-7242-2244-393

Denmark - Copenhagen
Tel: 45-4450-2828
Fax: 45-4485-2829

France - Paris
Tel: 33-1-69-53-63-20
Fax: 33-1-69-30-90-79

Germany - Munich
Tel: 49-89-627-144-0
Fax: 49-89-627-144-44

Italy - Milan
Tel: 39-0331-742611
Fax: 39-0331-466781

Netherlands - Drunen
Tel: 31-416-690399
Fax: 31-416-690340

Spain - Madrid
Tel: 34-91-708-08-90
Fax: 34-91-708-08-91

UK - Wokingham
Tel: 44-118-921-5869
Fax: 44-118-921-5820

01/02/08