SST-PFB3-104

Hardware Reference Guide

Document Edition: 1.0

Document #: 715-0079

Document Edition: 1.0

Date: November 18, 2004

This document applies to the SST-PFB3-104 interface card.

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Preface

Preface Sections:

- Purpose of this Guide
- Conventions

Warning

Only qualified electrical personnel familiar with the construction/ operation of this equipment and the hazards involved should install, adjust, operate, and/or service this equipment. Read and understand this guide in its entirety before proceeding. Failure to observe this precaution could result in severe bodily injury or, in extreme cases, loss of life.

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Purpose of this Guide

This guide contains technical and product-related information on the SST-PFB3-104 interface card and derivatives.

The SST-PFB3-104 has its own CPU that executes downloadable application firmware modules. The main function of these modules is to enable application-level product behavior. For more details, refer to the firmware reference guide.

Conventions

This guide uses stylistic conventions, special terms, and special notation to help enhance your understanding.

Style

The following stylistic conventions are used throughout this guide:

Bold	indicates field names, button names, tab names, and options or selections
Italics	indicates keywords or instances of new terms and/or specialized words that need emphasis
CAPS	indicates a specific key selection, such as ENTER, TAB, CTRL, ALT, DELETE
`Code Font`	indicates command line entries or text you would type into a field
Underlining	indicates a hyperlink
“>” delimiter	indicates how to navigate through a hierarchy of menu selections/options
“0x”	indicates a hexadecimal value

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Terminology

The following special terms are used throughout this guide:

Card	the SST-PFB3-104 network interface card
Firmware Module	the embedded software module that gets loaded to the card's memory and runs on the card. This is the operating system of the card, enabling it to respond to commands from the host and manage network communications.
Host	the computer system in which the card is installed
.ss3	an encrypted firmware module for the card

Special Notation

The following special notations are used throughout this guide:

Warning

Warning messages alert the reader to situations where personal injury may result. Warnings are accompanied by the symbol shown, and precede the topic to which they refer.

Caution

Caution messages alert the reader to situations where equipment damage may result. Cautions are accompanied by the symbol shown, and precede the topic to which they refer.

Note

A note provides additional information, emphasizes a point, or gives a tip for easier operation. Notes are accompanied by the symbol shown, and follow the text to which they refer.

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Contents

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1
Card Overview

Chapter Sections:

- Warnings and Cautions
- Card Features
- Hardware Description

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1.1 Warnings and Cautions

The card is an electrical component and must be treated with the following precautions:

Warning

Only qualified electrical personnel familiar with the construction/ operation of this equipment and the hazards involved should install, adjust, operate, and/or service this equipment. Read and understand this guide in its entirety before proceeding. Failure to observe this precaution could result in severe bodily injury or, in extreme cases, loss of life.

Warning

You must provide an external, hand-wired emergency stop circuit outside the programmable controller circuitry. This circuit must disable the system in case of improper operation. Uncontrolled machine motion may result if this procedure is not followed. Failure to observe this precaution could result in bodily injury.

Caution

The card contains static-sensitive components. Careless handling may severely damage the card. Do not touch any of the connectors or pins on the card. When not in use, the card should be stored in an anti-static bag. Failure to observe this precaution could result in damage to or destruction of the equipment.

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1.2 Card Features

The SST-PFB3-104 is the next-generation Profibus PC104 card. It can:

- Function as a DP Master
- Function as a DP Slave
- Function as a DPV1 Class1 & Class2 Master
- Send and receive FDL (layer 2) messages
- Support simultaneous operation in all of the above modes
- Support the standard Profibus baud rates of 9.6K, 19.2K, 31.25K, 45.45K, 93.75K, 187.5K, 500K, 1.5M, 3M and 12M

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1.3 Hardware Description

The main features of the card are described in more detail in the following sections.

Figure 1: The SST-PFB3-104 Interface Card

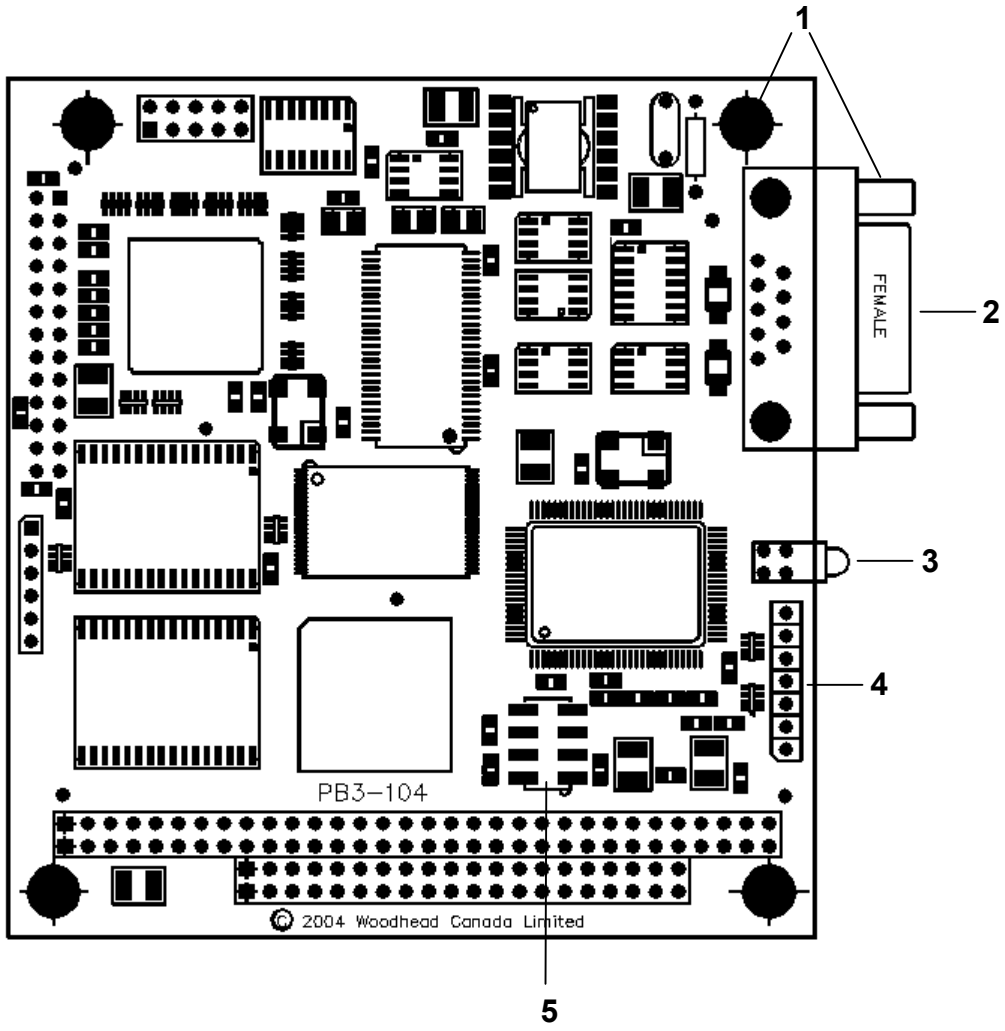

Table 1: Card Components

Feature	Description
1	Chassis Ground
2	DB9 Connector
3	LEDs
4	DIP Switch
5	LED Connector

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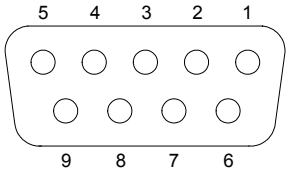
1.3.1 Chassis Ground

For the location of chassis ground, Refer to Figure 1: The SST-PFB3-104 Interface Card.

1.3.2 DB9 Connector

The card contains a standard Profibus DB9 female connector. Pin numbers are identified in the figure below.

Figure 2: The Profibus DB9 Female Connector



Note

The recommended male connector is the Brad Harrison PA9D01-42 Diagnostic D-Sub Connector.

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Selecting Cable

The recommended cable is Belden 3079A. Examples include:

- Brad Harrison 85-0001 PVR 2 conductor with shield, UL-listed Profibus cable
- Bosch Comnet DP #913 548 Flexible Profibus Cable
- Bosch Comnet DP #917 201 Trailing Profibus Cable
- Bosch Comnet DP #917 202 Massive Profibus Cable

Note

For instructions on connecting to a Profibus network, refer to Section 2.5, Connecting to a Profibus Network.

Using the Proper Line Type

Use this table to determine which line type best suits your system requirements.

Table 2: Line Types

Baud Rate (bits/s)	Line A Distance (Max)	Line B Distance (Max)	Total Capacitance of all Drop Cables
19.2k	1200 m**	1200 m**	*15nF
93.75k	1200 m**	1200 m**	*3nF
187.5k	1000 m**	600 m**	*1nF
500k	400 m**	200 m**	*0.6nF
1.5M	200 m**	N/A	*0.2nF
3, 6 and 12M	100 m**	N/A	*0.05nF
N/A = Not Applicable *If using a combination of both line types, divide the lengths shown by two **This is the sum of all bus segment and drop cable lengths			

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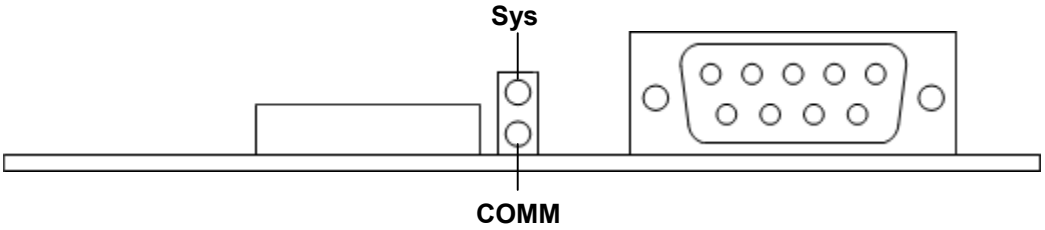
1.3.3 LEDs

The LEDs are illustrated in the following diagram and described below.

Figure 3: LEDs (Side View)



1.3.3.1 Sys LED

The Sys LED indicates the card's system status.

Table 3: Sys LED Behavior

LED State	Meaning
Off	Refer to the firmware reference guide
Green	Refer to the firmware reference guide
Red	Refer to the firmware reference guide
Amber	This is the default power-up state until the firmware module is running

1.3.3.2 COMM LED

The COMM LED indicates the card's communications status.

Table 4: COMM LED Behavior

LED State	Meaning
Off	Card is not online
Solid green	Card is online and scanning an active network
Flashing green	Card is online but not scanning
Red	Network error

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For a list of errors that can occur during power-up, refer to Section A.1.2, Fatal Hardware Self-Test Flash Codes. For runtime Sys LED behavior, refer to the firmware reference guide.

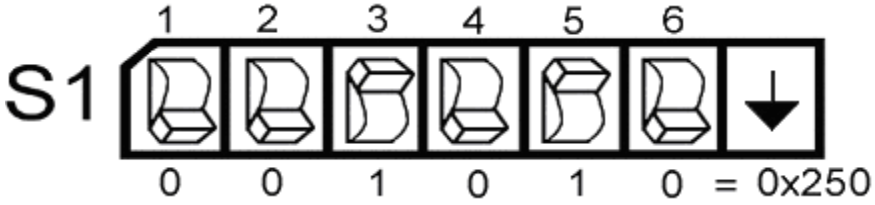
Note

For information on troubleshooting using LEDs, refer to Section 4.1, COMM LED is Red.

1.3.4 DIP Switch

The 6-position DIP switch is used to set the base I/O address for configuring the card.

Figure 4: DIP Switch



Note

Keep in mind that the card uses 8 I/O addresses. Selecting I/O address 250 actually uses I/O addresses 250 through 257.

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Table 5: DIP Switch Settings

A “1” in the following table indicates that a switch is *on* (or UP), and a “0” indicates that a switch is *off* (or DOWN). The arrow on the switch (refer to Figure 4: DIP Switch) indicates the direction in which a switch that’s *off* points.

Port Address Hex	1	2	3	4	5	6	Remarks
200	0	0	0	0	0	0	game port
208	0	0	0	0	0	1	
210	0	0	0	0	1	0	
218	0	0	0	0	1	1	
220	0	0	0	1	0	0	sound card
228	0	0	0	1	0	1	
230	0	0	0	1	1	0	
238	0	0	0	1	1	1	
240	0	0	1	0	0	0	
248	0	0	1	0	0	1	
250	0	0	1	0	1	0	Default
258	0	0	1	0	1	1	
260	0	0	1	1	0	0	
268	0	0	1	1	0	1	
270	0	0	1	1	1	0	
278	0	0	1	1	1	1	LPT2
280	0	1	0	0	0	0	
288	0	1	0	0	0	1	
290	0	1	0	0	1	0	
298	0	1	0	0	1	1	
2A0	0	1	0	1	0	0	
2A8	0	1	0	1	0	1	
2B0	0	1	0	1	1	0	
2B8	0	1	0	1	1	1	
2C0	0	1	1	0	0	0	
2C8	0	1	1	0	0	1	
2D0	0	1	1	0	1	0	
2D8	0	1	1	0	1	1	
2E0	0	1	1	1	0	0	
2E8	0	1	1	1	0	1	COM4
2F0	0	1	1	1	1	0	
2F8	0	1	1	1	1	1	COM2
600	1	0	0	0	0	0	Game port
608	1	0	0	0	0	1	
610	1	0	0	0	1	0	
618	1	0	0	0	1	1	

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Port Address Hex	1	2	3	4	5	6	Remarks
620	1	0	0	1	0	0	
628	1	0	0	1	0	1	
630	1	0	0	1	1	0	
638	1	0	0	1	1	1	
640	1	0	1	0	0	0	
648	1	0	1	0	0	1	
650	1	0	1	0	1	0	
658	1	0	1	0	1	1	
660	1	0	1	1	0	0	
668	1	0	1	1	0	1	
670	1	0	1	1	1	0	
678	1	0	1	1	1	1	LPT2
680	1	1	0	0	0	0	
688	1	1	0	0	0	1	
690	1	1	0	0	1	0	
698	1	1	0	0	1	1	
6A0	1	1	0	1	0	0	
6A8	1	1	0	1	0	1	
6B0	1	1	0	1	1	0	
6B8	1	1	0	1	1	1	
6C0	1	1	1	0	0	0	
6C8	1	1	1	0	0	1	
6D0	1	1	1	0	1	0	
6D8	1	1	1	0	1	1	
6E0	1	1	1	1	0	0	
6E8	1	1	1	1	0	1	COM4
6F0	1	1	1	1	1	0	
6F8	1	1	1	1	1	1	COM2

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1.3.5 LED Connector

The card contains an 8-pin LED connector. Pin numbers are identified in Figure 5 and Table 6. Table 7 identifies the external LED states and relevant voltage levels.

Figure 5: LED Connector

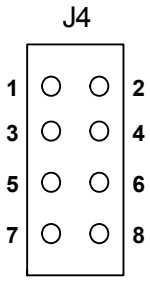

Table 6: Pin Names and Descriptions

Pin #	Pin Name	Description
1	N/A (reserved)	N/A
2	N/A (reserved)	N/A
3	LED_SG	Sys Green
4	LED_SR	Sys Red
5	LED_CG	Comm Green
6	LED_CR	Comm Red
7	GND	Ground
8	3V3	3.3 VDC power

Note

The maximum current for each pin is 24mA.

Table 7: External LED States

State	Level	
	LED_CR / LED_SR	LED_CG / LED_SG
LED is green	0	3V3
LED is red	3V3	0

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2
Installation

Chapter Sections:

- System Requirements
- Handling Precautions
- Installing the Card
- Downloading a Firmware Module
- Connecting to a Profibus Network

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2.1 System Requirements

To install and operate the card, the following system requirements must be met:

- Minimum 8K window in host memory map (maximum is 256K and default is 16K)
- An available PC104 slot
- If interrupts are required, you will need a physical interrupt

2.2 Handling Precautions

The card contains components that are sensitive to electrostatic discharge (ESD). Do not touch the card without following these precautions:

Caution

- Always follow correct ESD procedures before handling the card. We strongly recommend the use of a grounding wrist strap.
- Never touch any of the card's connectors or pins. Handle the card by its edges or bracket.
- When the card is not in your computer, always store it in its protective ESD bag.

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2.3 Installing the Card

This section describes the steps necessary to configure and install the card in your computer.

To install the card:

1. Ensure that all power to your computer is off.
2. Adequately ground yourself, as explained in Section 2.2, Handling Precautions.
3. Unplug the power cord, modem (if applicable), and any network cables.
4. Remove the computer cover. Consult your computer user's guide for information on installing add-in boards.
5. Set the DIP switch to the selected address (refer to Section 1.3.4, DIP Switch, for details).
6. Locate a compatible PC104 slot in your system.
7. Take the card out of its shipping container and anti-static bag, being careful not to touch any of the connectors or pins.
8. Slide the card into the slot and screw it down.

Note

Chassis ground connections in the computer may vary. For the card's chassis ground location, refer to Figure 1: The SST-PFB3-104 Interface Card.

9. Re-connect any items unplugged in Step 3.
10. Replace the computer cover and power up your computer.

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2.4 Downloading a Firmware Module

For instructions on downloading a firmware module to the card, refer to Section C.1, Loading a Firmware Module.

2.5 Connecting to a Profibus Network

This section provides connection, termination, power and grounding details.

2.5.1 Connecting the DB9

The following table describes how to connect the Profibus DB9.

Table 8: DB9 Instructions

DB9 Pin Description	DB9 Pin #	DB9 Termination with Card
Chassis ground	1	
Reserved	2	
Data +	3	Connect this pin to Pin 8 (data -) with 220 ohm resistor
Tx enable	4	
Isolated ground	5	Connect this pin to Pin 8 (data -) with 390 ohm resistor
Voltage plus	6	Connect this pin to Pin 3 (data +) with 390 ohm resistor
Reserved	7	
Data -	8	
Reserved	9	

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2.5.2 Termination

Always refer to the Profibus documentation for proper network termination and wiring directions.

2.5.3 Power

Profibus 5 VDC power is supplied by the card.

2.5.4 Grounding

Refer to the Profibus network documentation for grounding directions.

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3
Hardware Register Details

Chapter Sections:

- PFB3-104 Card Configuration Registers

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3.1 PFB3-104 Card Configuration Registers

This chapter provides technical hardware information. The following information is intended for programmers familiar with hardware-level PC programming.

3.1.1 Host Register Layout

The registers are located in I/O space. The base I/O address is set via the DIP switch.

Note

Upon card power up, or after a physical reset from the system, it typically takes 1 second for the card to initialize (though it is recommended that applications wait up to 2 seconds). Initialization can be confirmed by monitoring the LEDs or by reading the FamilyID register, as described in Section C.1.1, Verifying Card Presence.

Table 9: Host Register Layout

The following "offsets" are from the base address.

Offset	Name	7	6	5	4	3	2	1	0
00h	Control	CardRun (r/w)	MemEn (r/w)	IntEn (r/w)	WdTout (read)	HostIrq1 (r/w)	HostIrq0 (r/w)	CardIrq1 (r/w)	CardIrq0 (r/w)
01h	AddrMatch	AM19	AM18	AM17	AM16	AM15	AM14	AM13	AM12
02h	BankAddress	BA19	BA18	BA17	BA16	BA15	BA14	BA13	BA12
03h	WinSize	WS19	WS18	WS17	WS16	WS15	WS14	WS13	WS12
04h	HostIrq (r/w)	X	X	X	X	IrqLevel3	IrqLevel2	IrqLevel1	IrqLevel0
05	LedReg (read)	X	X	X	X	CommRed	CommGrn	SysRed	SysGrn
06h	Debug (r/w)	HWReset	X	X	JTAGEN	CPUTRST	CPUTMS	CPUTDI	CPUTCK
07	HDR (read)	HostDataReg (written by CPU)							

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3.1.2 Control Register

This register is a group of control and status bits.

Table 10: Control Register Settings

Bit	7	6	5	4	3	2	1	0
Name	CardRun	MemEn	IntEn	WdTout	HostIrq1	HostIrq0	CardIrq1	CardIrq0
Read/Write	R/W	R/W	R/W	R	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

The card has four interrupt flags, two for use in each direction. Setting CardIrq1 or CardIrq0 generates an interrupt to the card with the relevant flag set. When HostIrq1 OR HostIrq0 is '1' and IntEn is '1', the card drives the IRQ pin (as set by IrqLevel) high.

One flag could be used for a command interface, and another for changing I/O data. The firmware module dictates how these flags are used. If the module uses only one flag, it will be Flag 0.

Table 11: Control Register Bit Descriptions

Bit Name	Description
CardRun	This bit controls and indicates whether or not the card's processor is running. It also affects the Sys LED. • When this bit is 0, the processor is halted, and the LED is RED • When this bit is 1, the processor is running normally, and the LED is under card processor control • When this bit is 1, and watchdog has timed out, processor is halted, and the LED is RED • This bit must remain low for at least 50 μs to guarantee proper reset
MemEn	This bit indicates and controls whether or not the card's shared memory will respond to host memory accesses. This may be used to multiplex several SST-PFB3-104 cards at the same base address. MemEn high ('1') enables shared memory decoding of addresses in this board's range.
IntEn	• Writing 1 enables interrupts • Writing 0 disables interrupts (the HostIrq flags still function as described)
WdTout	WdTout high ('1') indicates that a watchdog timeout has occurred, or that the card's processor has been held in RESET by some other means. To restore this bit to 0, clear CardRun.
HostIrq1	• This bit is used by the card's processor to send interrupts to interrupt flag 1 of the host. • Writing 1 acknowledges the interrupt and clears it • Writing 0 has no effect • Reading 1 indicates interrupt in progress • Reading 0 indicates interrupt complete

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Bit Name	Description
HostIrq0	• This bit is used by the card's processor to send interrupts to interrupt flag 0 of the host. • Writing 1 acknowledges the interrupt and clears it • Writing 0 has no effect • Reading 1 indicates interrupt in progress • Reading 0 indicates interrupt complete
CardIrq1	This bit is used by the host to send interrupts to interrupt flag 1 of the card's processor. • Writing 1 generates an interrupt • Writing 0 has no effect • Reading 1 indicates interrupt in progress • Reading 0 indicates interrupt complete
CardIrq0	This bit is used by the host to send interrupts to interrupt flag 0 of the card's processor. • Writing 1 generates an interrupt • Writing 0 has no effect • Reading 1 indicates interrupt in progress • Reading 0 indicates interrupt complete

3.1.3 AddrMatch Register

This register controls the card's base memory address in host memory space.

Table 12: AddrMatch Register Settings

Bit	7	6	5	4	3	2	1	0
Name	AM19	AM18	AM17	AM16	AM15	AM14	AM13	AM12
Read/Write	R	R/W	R/W	R/W	R/W	R/W	R/W	R
Reset	1	0	0	0	0	0	0	0

Table 13: AddrMatch Register Values

Bit and Value								Hex	Address
AM19	AM18	AM17	AM16	AM15	AM14	AM13	AM12		
1	0	0	0	0	0	0	0	0x80	0x80000
1	0	0	0	0	0	1	0	0x82	0x82000
1	0	0	0	0	1	0	0	0x84	0x84000
1	0	0	0	0	1	1	0	0x86	0x86000
1	0	0	0	1	0	0	0	0x88	0x88000
1	0	0	0	1	0	1	0	0x8A	0x8A000
1	0	0	0	1	1	0	0	0x8C	0x8C000
1	0	0	0	1	1	1	0	0x8E	0x8E000
1	0	0	1	0	0	0	0	0x90	0x90000
1	0	0	1	0	0	1	0	0x92	0x92000

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Bit and Value								Hex	Address
AM19	AM18	AM17	AM16	AM15	AM14	AM13	AM12		
1	0	0	1	0	1	0	0	0x94	0x94000
1	0	0	1	0	1	1	0	0x96	0x96000
1	0	0	1	1	0	0	0	0x98	0x98000
1	0	0	1	1	0	1	0	0x9A	0x9A000
1	0	0	1	1	1	0	0	0x9C	0x9C000
1	0	0	1	1	1	1	0	0x9E	0x9E000
1	0	1	0	0	0	0	0	0xA0	0xA0000
1	0	1	0	0	0	1	0	0xA2	0xA2000
1	0	1	0	0	1	0	0	0xA4	0xA4000
1	0	1	0	0	1	1	0	0xA6	0xA6000
1	0	1	0	1	0	0	0	0xA8	0xA8000
1	0	1	0	1	0	1	0	0xAA	0xAA000
1	0	1	0	1	1	0	0	0xAC	0xAC000
1	0	1	0	1	1	1	0	0xAE	0xAE000
1	0	1	1	0	0	0	0	0xB0	0xB0000
1	0	1	1	0	0	1	0	0xB2	0xB2000
1	0	1	1	0	1	0	0	0xB4	0xB4000
1	0	1	1	0	1	1	0	0xB6	0xB6000
1	0	1	1	1	0	0	0	0xB8	0xB8000
1	0	1	1	1	0	1	0	0xBA	0xBA000
1	0	1	1	1	1	0	0	0xBC	0xBC000
1	0	1	1	1	1	1	0	0xBE	0xBE000
1	1	0	0	0	0	0	0	0xC0	0xC0000
1	1	0	0	0	0	1	0	0xC2	0xC2000
1	1	0	0	0	1	0	0	0xC4	0xC4000
1	1	0	0	0	1	1	0	0xC6	0xC6000
1	1	0	0	1	0	0	0	0xC8	0xC8000
1	1	0	0	1	0	1	0	0xCA	0xCA000
1	1	0	0	1	1	0	0	0xCC	0xCC000
1	1	0	0	1	1	1	0	0xCE	0xCE000
1	1	0	1	0	0	0	0	0xD0	0xD0000
1	1	0	1	0	0	1	0	0xD2	0xD2000
1	1	0	1	0	1	0	0	0xD4	0xD4000
1	1	0	1	0	1	1	0	0xD6	0xD6000
1	1	0	1	1	0	0	0	0xD8	0xD8000
1	1	0	1	1	0	1	0	0xDA	0xDA000
1	1	0	1	1	1	0	0	0xDC	0xDC000
1	1	0	1	1	1	1	0	0xDE	0xDE000
1	1	1	0	0	0	0	0	0xE0	0xE0000
1	1	1	0	0	0	1	0	0xE2	0xE2000
1	1	1	0	0	1	0	0	0xE4	0xE4000
1	1	1	0	0	1	1	0	0xE6	0xE6000
1	1	1	0	1	0	0	0	0xE8	0xE8000

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Bit and Value								Hex	Address
AM19	AM18	AM17	AM16	AM15	AM14	AM13	AM12		
1	1	1	0	1	0	1	0	0xEA	0xEA000
1	1	1	0	1	1	0	0	0xEC	0xEC000
1	1	1	0	1	1	1	0	0xEE	0xEE000
1	1	1	1	0	0	0	0	0xF0	0xF0000
1	1	1	1	0	0	1	0	0xF2	0xF2000
1	1	1	1	0	1	0	0	0xF4	0xF4000
1	1	1	1	0	1	1	0	0xF6	0xF6000
1	1	1	1	1	0	0	0	0xF8	0xF8000
1	1	1	1	1	0	1	0	0xFA	0xFA000
1	1	1	1	1	1	0	0	0xFC	0xFC000
1	1	1	1	1	1	1	0	0xFE	0xFE000

Table 14: AddrMatch Register Bit Descriptions

Bit Name	Description
AM19 – AM12	AM19-AM12 represent the upper address match required to decode memory. These bits select the base memory address, from 0xA0000 to 0xFE000. For example, writing 0xD0 to this register selects 0xD0000 as the memory base address. Refer to Table 13, AddrMatch Register Values, for more details. If a 16K window size is selected, AM13-AM12 are ignored and 16K boundaries are used for the memory address. As a result, only even-window boundaries may be chosen. The card could be set to 0xD0000 or 0xD4000, but 0xD2000 would be invalid. Refer to Table 19, Winsize Register Values, for information on bit usage with other window sizes.

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3.1.4 Bank Address Register

This register is used to switch banks of shared memory into host memory space.

Table 15: Bank Address Register Settings

Bit	7	6	5	4	3	2	1	0
Name	BA19	BA18	BA17	BA16	BA15	BA14	BA13	BA12
Read/Write	R	R	R/W	R/W	R/W	R/W	R/W	R
Reset	0	0	0	0	0	0	0	0

Table 16: Bank Address Register Values

In this table, the default window size is highlighted, and a value of "x" indicates "don't care".

Bit and Value								Window Size and Bank Number					
BA19	BA18	BA17	BA16	BA15	BA14	BA13	BA12	8k	16k	32k	64k	128k	256k
x	x	0	0	0	0	0	x	0	0	0	0	0	0
x	x	0	0	0	0	1	x	1	0	0	0	0	0
x	x	0	0	0	1	0	x	2	1	0	0	0	0
x	x	0	0	0	1	1	x	3	1	0	0	0	0
x	x	0	0	1	0	0	x	4	2	1	0	0	0
x	x	0	0	1	0	1	x	5	2	1	0	0	0
x	x	0	0	1	1	0	x	6	3	1	0	0	0
x	x	0	0	1	1	1	x	7	3	1	0	0	0
x	x	0	1	0	0	0	x	8	4	2	1	0	0
x	x	0	1	0	0	1	x	9	4	2	1	0	0
x	x	0	1	0	1	0	x	10	5	2	1	0	0
x	x	0	1	0	1	1	x	11	5	2	1	0	0
x	x	0	1	1	0	0	x	12	6	3	1	0	0
x	x	0	1	1	0	1	x	13	6	3	1	0	0
x	x	0	1	1	1	0	x	14	7	3	1	0	0
x	x	0	1	1	1	1	x	15	7	3	1	0	0
x	x	1	0	0	0	0	x	16	8	4	2	1	0
x	x	1	0	0	0	1	x	17	8	4	2	1	0
x	x	1	0	0	1	0	x	18	9	4	2	1	0
x	x	1	0	0	1	1	x	19	9	4	2	1	0
x	x	1	0	1	0	0	x	20	10	5	2	1	0
x	x	1	0	1	0	1	x	21	10	5	2	1	0
x	x	1	0	1	1	0	x	22	11	5	2	1	0
x	x	1	0	1	1	1	x	23	11	5	2	1	0
x	x	1	1	0	0	0	x	24	12	6	3	1	0

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Bit and Value								Window Size and Bank Number					
BA19	BA18	BA17	BA16	BA15	BA14	BA13	BA12	8k	16k	32k	64k	128k	256k
x	x	1	1	0	0	1	x	25	12	6	3	1	0
x	x	1	1	0	1	0	x	26	13	6	3	1	0
x	x	1	1	0	1	1	x	27	13	6	3	1	0
x	x	1	1	1	0	0	x	28	14	7	3	1	0
x	x	1	1	1	0	1	x	29	14	7	3	1	0
x	x	1	1	1	1	0	x	30	15	7	3	1	0
x	x	1	1	1	1	1	x	31	15	7	3	1	0

* x = don’t care

Table 17: Bank Address Register Bit Descriptions

Bit Name	Description
BA17-13	The card has 256k of memory accessible to the host. The Bank Address bits select which bank of memory the host can access. For example, in 16k mode, the bank number may be 0 through 15 (or 0x0 - 0xf). • The primary host interface window is located in bank 0 • BA17-BA13 represent the bank address, providing A17-A13 for shared RAM accesses • Bank numbers depend on the window size, which is selected using the WinSize bits. Refer to Table 19, Winsize Register Values, for more information.

To access any memory address in a flat address model, in any window size, set the Bank Address bits to correspond to address bits 19-12. In C, you would write:

```
outport( BankSelect, addr>>12);
offset= addr & ((inport( WinSize ) <<12 ) | 0x3FFF);
```


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3.1.5 WinSize Register

This register controls the window size by masking off the AM19-AM12 and BA19-12 bits in the AddrMatch and Bank Address registers. Table 19, Winsize Register Values, maps the WS bit values required for each valid window size.

Table 18: WinSize Register Settings

Bit	7	6	5	4	3	2	1	0
Name	WS19	WS18	WS17	WS16	WS15	WS14	WS13	WS12
Read/Write	R	R	R/W	R/W	R/W	R/W	R/W	R
Reset	0	0	0	0	0	0	1	1

Table 19: WinSize Register Values

In this table, the default window values are highlighted.

Bit and Value								Window Size	Description
WS19	WS18	WS17	WS16	WS15	WS14	WS13	WS12		
0	0	0	0	0	0	0	1	8K	AM19-AM13 used, AM12 ignored BA19-BA13 used, BA12 ignored
0	0	0	0	0	0	1	1	16K	AM19-AM14 used, AM13-AM12 ignored BA19-BA14 used, BA13-BA12 ignored
0	0	0	0	0	1	1	1	32K	AM19-AM15 used, AM14-AM12 ignored BA19-BA15 used, BA14-BA12 ignored
0	0	0	0	1	1	1	1	64K	AM19-AM16 used, AM15-AM12 ignored BA19-BA16 used, BA15-BA12 ignored
0	0	0	1	1	1	1	1	128K	AM19-AM17 used, AM16-AM12 ignored BA19-BA17 used, BA16-BA12 ignored
0	0	1	1	1	1	1	1	256K	AM19-AM18 used, AM17-AM12 ignored BA19-BA18 used, BA17-BA12 ignored

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Table 20: WinSize Register Bit Descriptions

Bit Name	Description
WS19-WS12	WS19-WS12 represent the window size, according to Table 19, Winsize Register Values. • Writing any value other than those above has no effect The size of the memory window affects the number of banks required to access all memory. Refer to Table 16: Bank Address Register Values, for more information.

3.1.6 HostIrq Register

This register controls how interrupts from the card are generated.

Table 21: HostIrq Register Settings

Bit	7	6	5	4	3	2	1	0
Name	Reserved				IrqLevel3	IrqLevel2	IrqLevel1	IrqLevel0
Read/Write	R	R	R	R	RW	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Table 22: HostIrq Register Bit Descriptions

Bit Name/ Value				Description
IrqLevel3-IrqLevel0				These bits determine the hardware interrupt level used when interrupts are enabled and an interrupt is generated by the card's processor. Supported values are:
0	0	1	0	IRQ 2
0	1	0	1	IRQ 5
0	1	1	1	IRQ 7
1	0	0	1	IRQ 9
1	0	1	0	IRQ 10
1	0	1	1	IRQ 11
1	1	0	0	IRQ 12
1	1	1	1	IRQ 15
Any other value is not supported, and causes hardware interrupts to be disabled.				

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3.1.7 LedReg Register

This register reflects the state of the LEDs, allowing host software to monitor the LEDs and display them on-screen.

Table 23: LedReg Register Settings

			COMM		Sys	
Bit	**7**	**6**	**5**	**4**	**1**	**0**
Name	Reserved		CommRed	CommGrn	SysRed	SysGrn
Read/Write	R	R	R	R	R	R
Reset	0	0	0	0	0	0

Table 24: LedReg Register Values

Bit Name/Value		Description
CommRed	**CommGrn**	These bits indicate the state of the communications LED.
0	0	Invalid
0	1	LED is green
1	0	LED is red
1	1	Invalid
SysRed	**SysGrn**	These bits indicate the state of the system LED
0	0	LED is off
0	1	LED is green
1	0	LED is red
1	1	LED is amber

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3.1.8 Debug Register

This register is reserved and must not be accessed by host applications.

3.1.9 HDR Register

The HDR register shall be used to pass 1 byte of data from the card to the host. The use of this register is determined by the firmware module/boot code. Refer to the firmware reference guide for details.

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4 Troubleshooting

Chapter Sections:

- COMM LED is Red
- Memory Conflict
- General Troubleshooting

For a list of hardware-related errors that can be generated by the card, refer to Section A.1, Card Errors.

Warning

Only qualified electrical personnel familiar with the construction and operation of this equipment and the hazards involved should install, adjust, operate, or service this equipment. Failure to observe this precaution could result in severe bodily injury or loss of life.

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4.1 COMM LED is Red

This section describes strategies for troubleshooting a red COMM LED.

Note

For information on LED flash codes, refer to Section A.1.2, Fatal Hardware Self-Test Flash Codes.

If the COMM LED is red, the card is not running or there has been a firmware run-time error. Check the WdTout bit (refer to Table 11, Control Register Bit Descriptions) to determine whether or not there has been a watchdog timeout, and consult the firmware reference guide. If you continue to experience difficulties, refer to Section 4.3, General Troubleshooting.

Note

The firmware module must be reloaded to restart the card.

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4.2 Memory Conflict

Examine the operating system's resource allocations. If the OS does not manage resources, review the requirements of other hardware installed in the machine to select a non-conflicting memory window.

If this does not solve the problem, make sure there is no shadow RAM at the same memory location as the card. You can do this in various ways, depending on the computer type, BIOS and other factors. If the computer has a plug and play BIOS, you may need to check the plug and play section.

Note

If you see a message stating, "Disable shadow ram...disable", this means that the disable of the shadow RAM is disabled. Some computers refer to this as *Video RAM*, and others do not allow you to access shadow RAM at all.

If the computer is plug and play, make sure there is an ISA window at the card's physical location. This window is often called an *ISA shared memory size* or *ISA shared memory base*, but there may be other variations.

If you continue to experience difficulties, refer to Section 4.3, General Troubleshooting.

4.3 General Troubleshooting

If you experience problems with the card:

1. Check the website at http://www.woodhead.com/ for technical notes.
2. Check the FAQs on the website.
3. Refer to Section E.3, Technical Support.

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A
Error Messages

Appendix Sections:

- Card Errors

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A.1 Card Errors

The following errors may be reported during the card's startup self-test.

A.1.1 HDR Messages

If HDR reads anything other than 0x41, the card hasn't been found. To fix the problem, follow these steps:

1. Double-check the switch settings and make sure they match up with the I/O driver port address setting in the host software application.
2. Make sure you have waited up to 2 seconds after the card reset has been negated before trying to access it.
3. Check for an I/O conflict.
4. If you continue to experience difficulties, refer to Section 4.3, General Troubleshooting.

Note

The default value for boot code is 0x41, but this can be changed by the firmware module. Refer to the firmware reference guide for more details.

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A.1.2 Fatal Hardware Self-Test Flash Codes

Fatal failures during startup are accompanied by an 8-bit fault code, flashed on the COMM LED. The fault code will be output MSB first, with a 1 (one) bit shown as a green LED, and a zero (0) bit shown as a red LED. This will occur for a period of 900ms, followed by 100ms of off time. The LSB will be followed by an additional 1000ms of off time, after which the sequence will repeat.

The following table describes each possible fault code. If you see any of these codes, contact Technical Support.

Table 25: LED Flash Codes

Value	Name	Description
0x01	BITTEST8	Bit test failure of an 8-bit memory range
0x02	BITTEST16	Bit test failure of a 16-bit memory range
0x03	BITTEST32	Bit test failure of a 32-bit memory range
0x04	ADDRTEST8	Address test failure of an 8-bit memory range
0x05	ADDRTEST16	Address test failure of a 16-bit memory range
0x06	ADDRTEST32	Address test failure of a 32-bit memory range
0x07-0x09	-	Reserved for future fatal start-up errors
0x10	JTAGFAILED	JTAG download failed
0x11	JTAG_ ERROR_UNKNOWN	JTAG programming error
0x12	JTAG_TDOMISMATCH	JTAG output data failed to match expected pattern
0x13	JTAG_MAXRETRIES	JTAG output data failed to match expected pattern after several attempts
0x14	JTAG_ILLEGALCMD	JTAG programming file contained an unknown/malformed command
0x15	JTAG_ERROR_ILLEGALSTATE	JTAG programming file commanded an illegal TAP state transition
0x16	JTAG_ERROR_DATAOVERFLOW	JTAG programming file contained a shift pattern in excess of MAX_LEN * 8 bits
0x20-0xFF	-	Reserved for firmware-specific fatal errors

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B
Technical Specifications

Appendix Sections

- Technical Specifications

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B.1 Technical Specifications

The following tables list the technical specifications for the card.

Table 26: Environmental Specifications

Ambient Conditions	Storage temp:	-40°C to +85°C
	Operating temp:	0°C to 50°C
	Humidity:	5% to 95% non-condensing
Typical Current Draw		600mA
PC104 Compliance		Compliant with PC/104 Specification Version 2.3

Table 27: Network Specifications

Isolation	1000V
Protocol	RS485
Data Rate	All Profibus data rates up to 12Mbps

Table 28: PC104 Bus Specifications

Dimensions	Height:	3.775 inches
	Width:	3.550 inches
Resources		• PC104 Memory Region = 256K of 16-bit PC104 memory • PC104 I/O Region = 8 bytes of PC104 I/O memory • One PC104 interrupt

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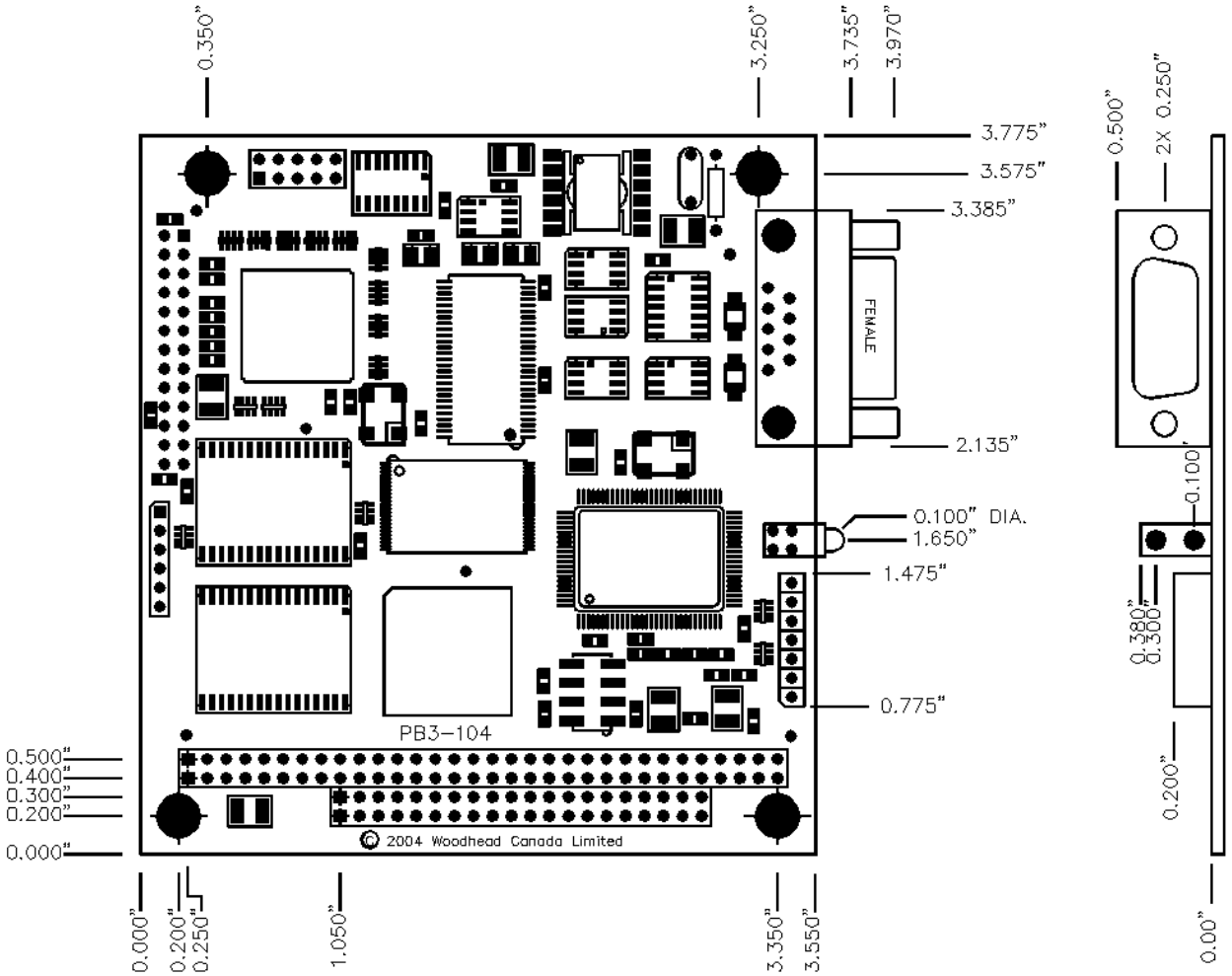
Figure 6: Card Dimensions



For information on card components, refer to Section 1.3, Hardware Description.

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C
Loading a Firmware Module

Appendix Sections:

- Loading a Firmware Module

Note

This appendix describes how to load the card manually, or how to write your own loader.

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C.1 Loading a Firmware Module

Firmware modules for the card are supplied as .ss3 files, found on the software CD-ROM or on the website at http://www.woodhead.com/.

If you are developing a driver for the card or producing a stand-alone embedded application, the following section describes the basic sequence of steps to manually load a firmware module onto the card.

Note

For register descriptions, refer to Chapter 3, Hardware Register Details.

C.1.1 Verifying Card Presence

To verify the card's presence, follow these steps:

1. Start up your computer.
2. Following release of the backplane reset, wait at least 1 second (though 2 is recommended).
3. Verify a Control Register value of 0x41.
4. If HDR reads anything other than 0x41, the card is still in Reset or has not been found. Double-check that the Short I/O address matches the DIP Switch setting. If you continue to experience difficulties, contact technical support (refer to Section E.3, Technical Support, for details).

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C.1.2 Checking for Conflicting RAM

Before the card's shared memory can be safely enabled, it must be determined that no other devices in the system are using the intended memory address range.

Note

Any task switching, interrupts or processes should be disabled during this procedure.

To check for conflicting RAM, follow these steps:

1. Write zero (0) to the Control Register to disable the card.
2. Read a word from the target memory window and save it.
3. Write 0xAA55 to the target address.
4. Read the target address. It should not contain 0xAA55.
5. If 0xAA55 is read, a conflict exists. Perform the following steps:
   - Restore the saved value to the target address
   - Abort the load procedure
   - Examine the resource allocations in your operating system. If your OS does not manage resources, review the requirements of the other hardware installed in your machine to select a non-conflicting memory window. If you continue to experience difficulties, contact technical support (refer to Section E.3, Technical Support, for details).

Note

If you are unsure of the system's memory usage, you may want to do a full memory window verification to ensure that there are no memory conflicts.

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C.1.3 Testing Card RAM

To test the card's RAM, follow these steps:

1. Write the upper byte of the desired 20-bit base address to the AddrMatch Register.
2. Write the desired window size to the WinSize register (refer to Section 3.1.5, WinSize Register, for details). The default value in the window size is 0x3F.
3. Write 0x40 (MemEn) to the Control Register at offset 1.
4. Fill the shared memory with a test pattern.

Note

We recommend using a test pattern with a unique value for each word in a given bank. In C, this could be:

```
~offset + bank.
```

5. Repeat steps 3-4 for all memory banks.
6. Verify the test pattern.

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C.1.4 Loading and Starting the Firmware Module

To load and start the firmware module, follow these steps:

1. Write the contents of the entire firmware file into shared memory, starting at bank zero (0), offset zero (0).

2. If the application requires interrupts from the card, write the interrupt ID to the HostIrq Register and bit-wise OR value 0x20 (IntEn) to the Control Register.

3. Bit-wise OR the value 0x80 (CardRun) to the Control Register to start the firmware module.

4. Start a 2-second timeout timer and wait for bit 2 (HostIrq0) in the Control Register to set.

5. If the timer expires, the firmware module failed to start. Write zero to the Control Register to disable the card. If this problem persists, contact Technical Support for assistance.

6. Check the load status, as per the firmware reference guide.

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D
CE Compliance

Appendix Sections:

- CE Compliance

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D.1 CE Compliance

This device meets or exceeds the requirements of the following standard:

- EN 61326:1998 including amendments A1 and A2: - Class A - “Electrical equipment for measurement, control and laboratory use - EMC requirements.”

Warning

This is a Class A product. In a domestic environment this product may cause radio interference in which case you may be required to take adequate measures.

Caution

This equipment is neither designed for, nor intended for operation in installations where it is subject to hazardous voltages and hazardous currents.

Marking of this equipment with the symbol CE indicates compliance with European Council Directive 89/336/EEC - The EMC Directive as amended by 92/31/EEC and 93/68/EEC.

Note

To maintain compliance with the limits and requirements of the EMC Directive, it is required to use quality interfacing cables and connectors when connecting to this device. Refer to the cable specifications in the Hardware Guide for selection of cable types.

Note

The backplane voltage supply for this equipment must be delivered as Separated Extra Low Voltage (SELV).

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E

Warranty and Support

Appendix Sections:

- Warranty
- Reference Documents
- Technical Support

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E.1 Warranty

For warranty information pertaining to the card, refer to http://www.mysst.com/warranty.asp.

E.2 Reference Documents

PC/104 Specification Version 2.3, June 1996.

E.3 Technical Support

Please ensure that you have the following information readily available before calling for technical support:

- Card type and serial number
- Computer's make, model and hardware configuration (other cards installed)
- Operating system type and version
- Details of the problem you are experiencing: firmware module type and version, target network and circumstances that may have caused the problem

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E.3.1 Getting Help

Technical support is available during regular business hours by telephone, fax or email from any Woodhead Software & Electronics office, or from http://www.woodhead.com/. Documentation and software updates are also available on the website.

Note

If you are using the card with a third-party application, refer to the documentation for that package for information on configuring the software for the card.

North America

Canada:
Tel: 1-519-725-5136
Fax: 1-519-725-1515
Email: techsupportna@woodhead.com

Europe

France:
Tel: 33-(0)2-32-96-04-22
Fax: 33-(0)2-32-96-04-21
Email: supportfr@applicom-int.com

Germany:
Tel: 49-711-782-374-22
Fax: 49-711-782-374-11
Email: supportde@applicom-int.com

Italy:
Tel: 39-01-059-540-52
Fax: 39-0-10-59-56-925
Email: supportit@applicom-int.com

United Kingdom:
Tel: 33-(0)2-32-96-04-23
Fax: 44-161-285-8686
Email: supportintl@applicom-int.com

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Tel: 81-452-24-3560
Fax: 81-52-745-7622
Email: techsupport@woodhead.co.jp

Singapore:
Tel: 65-64-67-96-52
Fax: 65-6261-3588
Email: info@woodhead.com.sg

China:
Tel: 86-21-5032-8080
Fax: 86-21-5031-8833
Email: techsupport@woodhead.co.jp

For the most current contact details, please visit http://www.woodhead.com/.

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Index

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