Woodhead

SST-DN3-VME-1, 2 and 4

Hardware Reference Guide

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This document applies to the SST-DN3-VME-1, SST-DN3-VME-2 and SST-DN3-VME-4 interface cards.

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Preface

Preface Sections:

- Purpose of this Guide

- Conventions

 Warning

Only qualified electrical personnel familiar with the construction/ operation of this equipment and the hazards involved should install, adjust, operate, and/or service this equipment. Read and understand this guide in its entirety before proceeding. Failure to observe this precaution could result in severe bodily injury or, in extreme cases, loss of life.

Purpose of this Guide

This guide contains technical and product-related information on the SST-DN3-VME-1, SST-DN3-VME-2 and SST-DN3-VME-4 network interface cards.

The SST-DN3-VME-1 consists of a single DeviceNet network interface (or *channel*), and the SST-DN3-VME-2 and 4 each comprise independent interfaces, controlled by independent CPUs. Each CPU executes downloadable application firmware modules, which enable application-level product behavior. For more details, refer to relevant Firmware Reference Guide.

> **Note**
>
> An application running on one channel does not affect the performance of other channels, as it does not share memory or processor resources with them.

> **Note**
>
> In this manual, the SST-DN3-VME-1, SST-DN3-VME-2 and SST-DN3-VME-4 will be referred to as the *card*, except where product differences apply.

Conventions

This guide uses stylistic conventions, special terms, and special notation to help enhance your understanding.

Style

The following stylistic conventions are used throughout this guide:

Bold	indicates field names, button names, tab names, and options or selections
Italics	indicates keywords (indexed) or instances of new terms and/or specialized words that need emphasis
CAPS	indicates a specific key selection, such as ENTER, TAB, CTRL, ALT, DELETE
`Code Font`	indicates command line entries or text that you would type into a field
<u>Underlining</u>	indicates a hyperlink
">" delimiter	indicates how to navigate through a hierarchy of menu selections/options
"0x" or "-H"	indicates a hexadecimal value

Terminology

The following special terms are used throughout this guide:

Card	the SST-DN3-VME-1, SST-DN3-VME-2 or SST-DN3-VME-4 network interface card
Channel	a DeviceNet network interface on the card
Firmware Module	the embedded software module that gets loaded to the card's memory and runs on the card. This is the operating system of the card, enabling it to respond to commands from the host and manage network communications.
Host	the computer system in which the card is installed
.bin	an unencrypted firmware module for the card
.ss3	an encrypted firmware module for the card

Special Notation

The following special notations are used throughout this guide:

Warning

Warning messages alert the reader to situations where personal injury may result. Warnings are accompanied by the symbol shown, and precede the topic to which they refer.

Caution

Caution messages alert the reader to situations where equipment damage may result. Cautions are accompanied by the symbol shown, and precede the topic to which they refer.

Note

A note provides additional information, emphasizes a point, or gives a tip for easier operation. Notes are accompanied by the symbol shown, and follow the text to which they refer.

Contents

1
Card Overview

Chapter Sections:

- Warnings and Cautions

- Card Features

- Byte Ordering

- Hardware Description

1.1 Warnings and Cautions

The card is an electrical component and must be treated with the following precautions:

Warning

Only qualified electrical personnel familiar with the construction/ operation of this equipment and the hazards involved should install, adjust, operate, and/or service this equipment. Read and understand this guide in its entirety before proceeding. Failure to observe this precaution could result in severe bodily injury or, in extreme cases, loss of life.

Warning

You must provide an external, hand-wired emergency stop circuit outside the programmable controller circuitry. This circuit must disable the system in case of improper operation. Uncontrolled machine motion may result if this procedure is not followed. Failure to observe this precaution could result in bodily injury.

Caution

The card contains static-sensitive components. Careless handling may severely damage the card. Do not touch any of the connectors or pins on the card. When not in use, the card should be stored in an anti-static bag. Failure to observe this precaution could result in damage to or destruction of the equipment.

Caution

Do not insert or remove cards from the system with DeviceNet power applied. Card damage may result.

1.2 Card Features

The card is a VME interface for communication with DeviceNet networks. Each channel has:

- A 16-bit VME interface, compliant with VME, VITA 1.1 (1997). 16 bits is the width of the data bus and does not restrict the card from being used in a 32-bit operating system.

- 66 MHz ColdFire Processor

- 256 KB of shared RAM

- DeviceNet-compliant 5-pin CAN connector

- Data rate of up to 1 Mbaud for CAN, and 125K, 250K and 500K for DeviceNet

- Bi-color LEDs showing card status

- Isolated physical layer

> **Note**
>
> Applications running on one channel do not affect the performance of other channels and do not share memory or processor resources with other channels.

1.3 Byte Ordering

The card uses Intel-style (little endian) byte ordering for multi-byte entities LSB-low address and MSB-high address. If your host system uses Motorola (big endian) byte ordering (MSB-low address and LSB-high address), you must compensate for byte ordering in software.

The following language macro will compensate for byte ordering in a 16-bit data entity:

#define SWAP_WORD (WordData) ((WordData<<8) | (WordData>>8))

1.4 Hardware Description

The main features of the card are described in more detail in the following sections.

Figure 1:   The SST-DN3-VME-1, 2 and 4 Interface Card
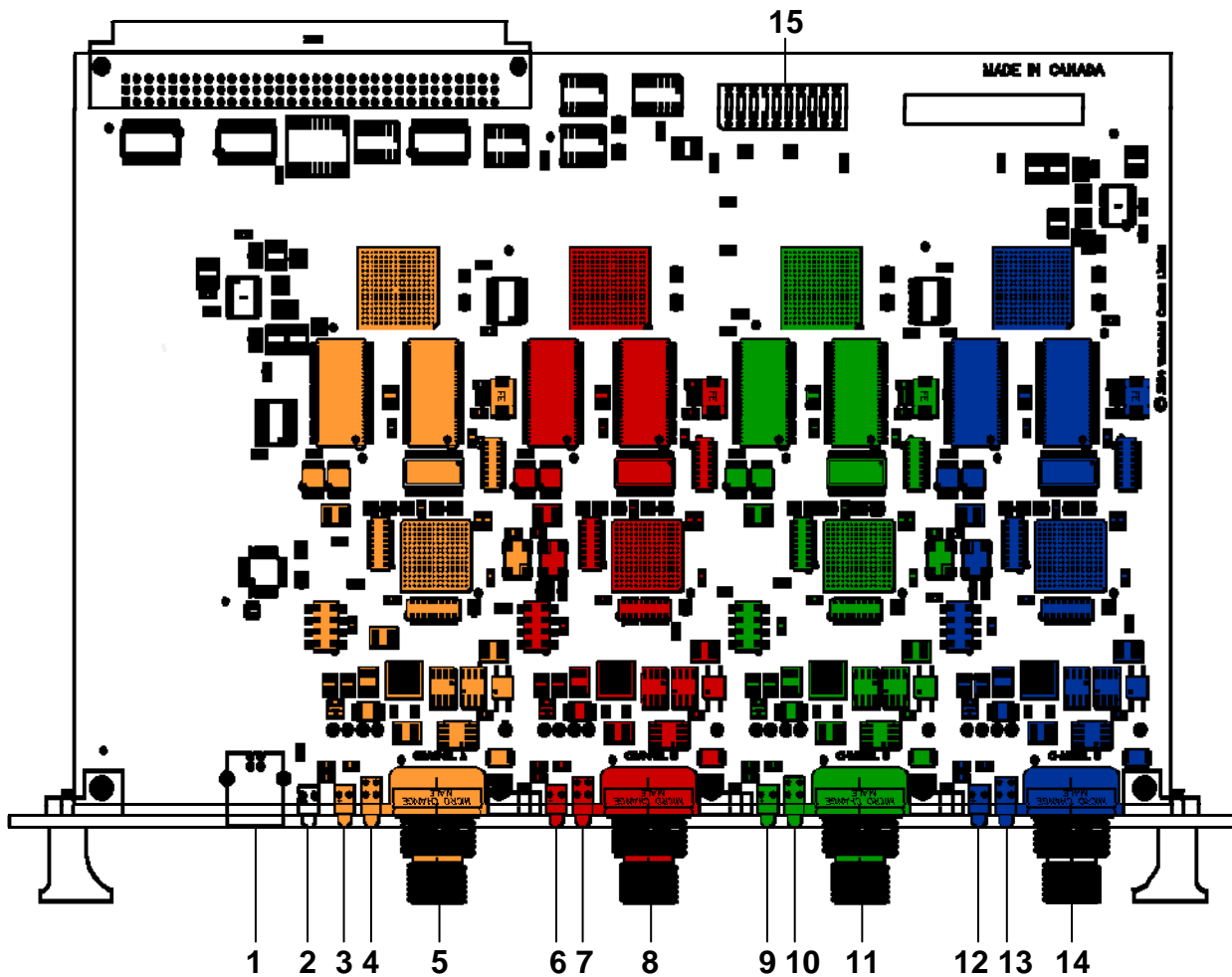
Table 1:   Component Names

Component	Description
1	USB Port
2	VME Status LED
3	Channel A DeviceNet Power Status LED
4	Channel A Health and Comm LEDs
5	Channel A M12 Connector
6	Channel B DeviceNet Power Status LED
7	Channel B Health and Comm LEDs
8	Channel B M12 Connector
9	Channel C DeviceNet Power Status LED
10	Channel C Health and Comm LEDs
11	Channel C M12 Connector
12	Channel D DeviceNet Power Status LED
13	Channel D Health and Comm LEDs
14	Channel D M12 Connector
15	Dip Switch

Legend

Shared components

Channel A

Channel B

Channel C

Channel D
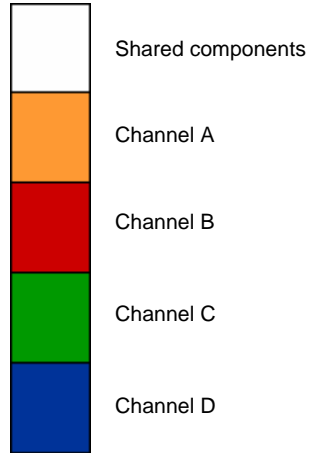
1.4.1 USB Port

The card's USB port allows the network configuration file and firmware module to be transferred to flash, and for named firmware to start automatically on reset.

The first time you plug it in, you will be prompted to select a driver. Browse to the installation CD and select **wseusb.inf**. After that, the USB port will start automatically when you go online.

Figure 2:   USB Port
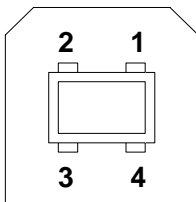
Table 2:   Pin Names and Descriptions

Pin #	Pin Name	Description
1	+5	USB power. Not used.
2	-Data	Data pin.
3	+Data	Data pin.
4	GND	USB ground.

Note

The recommended USB cable is USB A-D Cable M/M, USB A Male and USB B Male.

For information on plugging in the USB port and using the BIOS utility, refer to Section A.1, USB Port Operation.

1.4.2 LEDs

The LEDs are illustrated in the following diagram and described below.

Figure 3:   Assembled Mounting Bracket – Front View
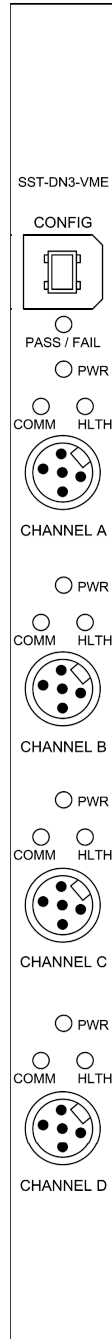
1.4.2.1 Pass/Fail Status LED

The Pass/Fail Status LED indicates the system's status.

Table 3:   Status LED Behavior

LED State	Meaning
Green	This is the default power-up state. If the SysFail bit in the VME register is set to a logic "1", the LED will turn red.
Red	An error has occurred in the system. The system fail signal is asserted on the backplane.

1.4.2.2 Power LED

The PWR LED is an indicator that represents whether or not power is applied to the CAN connector. The PWR LED's behavior is described in the following table:

Table 4:   PWR LED Behavior

Color	Status
Green	CAN bus power present
Red	CAN bus power not present
Off	VME power not present

1.4.2.3 Comm LED

The COMM LED indicates the communications status of each channel on the card.

Table 5:   COMM LED Behavior

LED State	Meaning
Off	Channel is not online
Solid green	Channel is online and scanning an active network
Flashing green	Channel is online but not scanning
Red	Network error

1.4.2.4 Health LED

The Health LED indicates the status of each channel on the card.

Table 6:   HLTH LED Behavior

LED State	Meaning
Off	VME power not present
Green	Firmware module loaded and running
Amber	Bootcode running. Firmware module not loaded
Red	Firmware module not loaded, an error occurred during the load, or a runtime fatal error occurred

For a list of errors that can occur during power-up, refer to Section A.2.2, Fatal Hardware Self-Test Flash Codes. For runtime Health LED behavior, refer to the Firmware Reference Guide.

Note

For information on troubleshooting using LEDs, refer to Section 4.1, COMM LED is Red.

1.4.3 M12 Connector

The DeviceNet network connector is an M12 (Micro) connector. The following diagram illustrates the pin numbers and names.

Figure 4:   M12 Connector (Male)
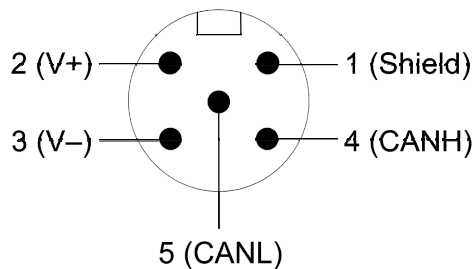
1.4.3.1 V+, V-

These are the DeviceNet network power supply terminals. Refer to the DeviceNet Specification for power supply ratings and further information.

1.4.3.2 CANH, CANL

These are the CAN communication bus terminals. Refer to the DeviceNet Specification for more information on cable specifications.

1.4.3.3 SHIELD

Connect the network cable shield to this terminal. The shield is snubbed to the PC chassis ground, and should be connected directly to earth ground at only one point in the network.

Note

For instructions on connecting to a CAN or DeviceNet network, refer to Section 2.5, Connecting to a Network.

1.4.4 LED Connector

The card contains an 8-pin LED connector. Pin numbers are identified in Figure 5 and Table 7. Table 8 identifies the external LED states and relevant voltage levels.

Figure 5:   LED Connector

```
      J4
   ┌─────────┐
 1 │  ○   ○  │ 2
 3 │  ○   ○  │ 4
 5 │  ○   ○  │ 6
 7 │  ○   ○  │ 8
   └─────────┘
```
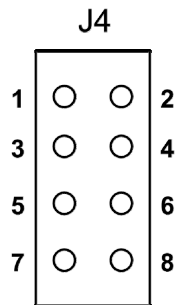
Table 7:   Pin Names and Descriptions

Pin #	Pin Name	Description
1	LED_PG	Power Green
2	LED_PR	Power Red
3	LED_HG	Health Green
4	LED_HR	Health Red
5	LED_CG	Comm Green
6	LED_CR	Comm Red
7	GND	Ground
8	3V3	3.3 VDC power

Note

The maximum current for each pin is 24mA.

Table 8:   External LED States

State	Level	
	LED_PR / LED_CR / LED_HR	LED_PG / LED_CG / LED_HG
LED is green	0	3V3
LED is red	3V3	0

1.4.5 DIP Switch (S1)

The card has a 10-position DIP switch that must be set before the card is installed. The DIP switch is used to set the base I/O address used to configure the card.

Figure 6:   DIP Switch (Shown in Off Position)
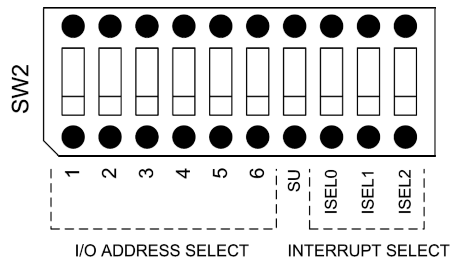
Table 9:   Switch Positions and Settings

Position	Purpose
1-6	Short I/O address
7	Access privilege
8-10	Interrupt

1.4.5.1 Setting the Short I/O Base Address

The 1 Kbyte block of short address space occupied by the card is located on a 1 Kbyte boundary at an address selected by positions 1 through 6 of the switch. These switch positions correspond to address bits A15 through A10, respectively. For example, when all switches are ON, the base address for Channel A is 0x0000, Channel B is 0x100, Channel C is 0x200 and Channel D is 0x300.

Table 10:   Positions 1 Through 6

Position	Channel A/B Corresponding Address Line
1	A15
2	A14
3	A13
4	A12
5	A11
6	A10

Note

On a 1-channel card, selecting I/O address 0x0 actually uses 0x0 through 0xFF; on a 2-channel card, it uses 0 through 0x1FF, and on a 4-channel card, it uses 0x0 through 0x3FF.

Note

Switches 1-6 represent the card's short I/O base address.

Table 11:   DIP Switch Offsets

The 4 channels shall be offset in 0x100 increments such that Switch Setting + Offset = Channel Location:

Short Address Space Offset	CH-A	CH-B	CH-C	CH-D
0X0000	✔			
0X0100		✔		
0X0200			✔	
0X0300				✔

Table 12:   DIP Switch Settings

In the following table, ON indicates that the switch is up, and OFF indicates that it is down.

Short Address Channel A	SW1-6 (A15-A10)					
	1 A15	2	3	4	5	6 A10
0x0000	ON	ON	ON	ON	ON	ON
0x0400	ON	ON	ON	ON	ON	OFF
0x0800	ON	ON	ON	ON	OFF	ON
0x0C00	ON	ON	ON	ON	OFF	OFF
0x1000	ON	ON	ON	OFF	ON	ON
0x1400	ON	ON	ON	OFF	ON	OFF
0x1800	ON	ON	ON	OFF	OFF	ON
0x1C00	ON	ON	ON	OFF	OFF	OFF
0x2000	ON	ON	OFF	ON	ON	ON
0x2400	ON	ON	OFF	ON	ON	OFF
0x2800	ON	ON	OFF	ON	OFF	ON
0x2C00	ON	ON	OFF	ON	OFF	OFF
0x3000	ON	ON	OFF	OFF	ON	ON
0x3400	ON	ON	OFF	OFF	ON	OFF
0x3800	ON	ON	OFF	OFF	OFF	ON
0x3C00	ON	ON	OFF	OFF	OFF	OFF
0x4000	ON	OFF	ON	ON	ON	ON
0x4400	ON	OFF	ON	ON	ON	OFF
0x4800	ON	OFF	ON	ON	OFF	ON
0x4C00	ON	OFF	ON	ON	OFF	OFF
0x5000	ON	OFF	ON	OFF	ON	ON
0x5400	ON	OFF	ON	OFF	ON	OFF
0x5800	ON	OFF	ON	OFF	OFF	ON
0x5C00	ON	OFF	ON	OFF	OFF	OFF

Short Address Channel A	SW1-6 (A15-A10)					
	1 A15	2	3	4	5	6 A10
0x6000	ON	OFF	OFF	ON	ON	ON
0x6400	ON	OFF	OFF	ON	ON	OFF
0x6800	ON	OFF	OFF	ON	OFF	ON
0x6C00	ON	OFF	OFF	ON	OFF	OFF
0x7000	ON	OFF	OFF	OFF	ON	ON
0x7400	ON	OFF	OFF	OFF	ON	OFF
0x7800	ON	OFF	OFF	OFF	OFF	ON
0x7C00	ON	OFF	OFF	OFF	OFF	OFF
0x8000	OFF	ON	ON	ON	ON	ON
0x8400	OFF	ON	ON	ON	ON	OFF
0x8800	OFF	ON	ON	ON	OFF	ON
0x8C00	OFF	ON	ON	ON	OFF	OFF
0x9000	OFF	ON	ON	OFF	ON	ON
0x9400	OFF	ON	ON	OFF	ON	OFF
0x9800	OFF	ON	ON	OFF	OFF	ON
0x9C00	OFF	ON	ON	OFF	OFF	OFF
0xA000	OFF	ON	OFF	ON	ON	ON
0xA400	OFF	ON	OFF	ON	ON	OFF
0xA800	OFF	ON	OFF	ON	OFF	ON
0xAC00	OFF	ON	OFF	ON	OFF	OFF
0xB000	OFF	ON	OFF	OFF	ON	ON
0xB400	OFF	ON	OFF	OFF	ON	OFF
0xB800	OFF	ON	OFF	OFF	OFF	ON
0xBC00	OFF	ON	OFF	OFF	OFF	OFF
0xC000	OFF	OFF	ON	ON	ON	ON
0xC400	OFF	OFF	ON	ON	ON	OFF
0xC800	OFF	OFF	ON	ON	OFF	ON
0xCC00	OFF	OFF	ON	ON	OFF	OFF
0xD000	OFF	OFF	ON	OFF	ON	ON
0xD400	OFF	OFF	ON	OFF	ON	OFF
0xD800	OFF	OFF	ON	OFF	OFF	ON
0xDC00	OFF	OFF	ON	OFF	OFF	OFF
0xE000	OFF	OFF	OFF	ON	ON	ON
0xE400	OFF	OFF	OFF	ON	ON	OFF
0xE800	OFF	OFF	OFF	ON	OFF	ON
0xEC00	OFF	OFF	OFF	ON	OFF	OFF
0xF000	OFF	OFF	OFF	OFF	ON	ON
0xF400	OFF	OFF	OFF	OFF	ON	OFF
0xF800	OFF	OFF	OFF	OFF	OFF	ON
0xFC00	OFF	OFF	OFF	OFF	OFF	OFF

1.4.5.2 Access Privileges

The card provides 8-bit access to objects in the short address space and 8- and 16-bit access to objects in the standard address space. The VME master selects whether a particular bus cycle accesses short, standard, extended, or long (extended and long are not used on the card) address spaces, and the type of access, through the use of the address modifier codes. The card decodes these address modifier codes and determines the object to be accessed.

In addition to selecting one of four spaces available on the VMEbus, address modifier codes also select:

- Whether the master is making a supervisory or non-privileged access

- Whether the access is to program or data space (for all but short address space accesses)

- Whether it is to be a single-object or block access

The card can respond to address modifier codes 0x03D, 0x039, 0x02D, and 0x029. Supervisory or non-privileged data accesses may be made to standard address space (0x03D and 0x039 respectively). Supervisory or non-privileged accesses may be made to short address space (0x02D and 0x029 respectively). An access to the card with an address modifier code that is not supported causes a VMEbus error.

Position 7 of the card's DIP switch selects whether only supervisory accesses or both supervisory and non-privileged accesses are permitted. The following table shows the switch positions.

Table 13:   Access Privileges (Non-Privileged)

Address Modifier	Description	Support
0x29	Short non-privileged data access (A16 mode)	D08(Odd) supported if SW7 is on.
0x2d	Short supervisory data access (A16 mode)	D08(Odd) supported.
0x39	Standard non-privileged data access (A24 mode)	D08(EvenOdd) and D16 supported if SW7 is on.
0x3d	Standard supervisory data access (A24 mode)	D08(EvenOdd) and D16 supported.

Configuration signal position 7 (non-priv) must be 1 (TTL 5V) to enable non-privileged accesses.

Table 14:   Switch S1-Position 7

Position	Permitted Access
ON	Non-privileged
OFF	Supervisory only

⚠ Caution

If the host makes a non-privileged access to the card when this switch is in the supervisory only position, a VMEbus error occurs.

1.4.5.3 Interrupts

The card can generate and acknowledge interrupts on any one of VMEbus interrupt lines 1 through 7 (or none). The interrupt level is selected by positions 8 through 10 of switch S1, as detailed below:

Table 15:   Switch Positions 8 through 10

SW8-10			VME Interrupt Level
8	**9**	**10**	
ON	ON	ON	None. Interrupts may be detected by polling IRQ bits in Control register (Card Offset + 0x01)
OFF	ON	ON	1
ON	OFF	ON	2
OFF	OFF	ON	3
ON	ON	OFF	4
OFF	ON	OFF	5
ON	OFF	OFF	6
OFF	OFF	OFF	7

The card interrupter is a ROAK (release-on-acknowledge) type. The interrupt request is removed from the VMEbus when the card responds to an interrupt acknowledge. However, the Card-IRQ bit in the Control register remains set until cleared by the host.

1.4.5.4 Default Switch Settings

The card is shipped with all switches ON. This corresponds to:

- Short I/O address 0000

- Supervisory and non-privileged access permitted

- Interrupts disabled

2

Hardware Installation

Chapter Sections:

- System Requirements

- Handling Precautions

- Installing the Card

- Downloading a Firmware Module

- Connecting to a Network

2.1 System Requirements

To install and operate the card, the following system requirements must be met:

- A controller that conforms to VMEbus spec VME64 (VITA 1.1 1997)

- Minimum 16K window, located on a 64k boundary in VME standard space

- The ability to generate and accept 16-bit data transfers (VME D16) with both VME A24 standard address and VME A16 short I/O address transfers

- If interrupts are required, you will need a physical interrupt. On multiple-channel cards, this will be shared between channels.

2.2 Handling Precautions

The card contains components that are sensitive to electrostatic discharge (ESD).
Do not touch the card without following these precautions:

⚠ Caution

- Always follow correct ESD procedures before handling the card.
  We strongly recommend the use of a grounding wrist strap.
- Never touch any of the card's connectors or pins. Handle the card by its edges or bracket.
- When the card is not in your computer, always store it in its protective anti-static bag.

⚠ Caution

Do not insert or remove cards from the system with DeviceNet power applied. Card damage may result.

2.3 Installing the Card

This section describes the steps necessary to configure and install the card in your computer.

To install the card in your computer:

1. Ensure that all power to your computer is off.

2. Adequately ground yourself, as explained in Section 2.2, <u>Handling Precautions</u>.

3. Unplug the power cord, modem (if applicable), and any network cables.

4. Remove the computer cover. Consult your computer user's guide for information on installing add-in boards.

5. Take the card out of its shipping container and anti-static bag, being careful not to touch any of the connectors or pins.

6. Set the DIP switch to the selected short I/O address (refer to Section 1.4.5.1, <u>Setting the Short I/O Base Address</u>, for details).

7. Firmly press the card on to the VME connector.

8. Secure the card using the screws provided.

9. Replace the computer cover.

10. Re-connect any items unplugged in Step 3.

2.4 Downloading a Firmware Module

For instructions on downloading a firmware module to the card, refer to Section C.1, Loading a Firmware Module.

2.5 Connecting to a Network

This section is divided into two parts: connecting to a DeviceNet network, and connecting to a CAN network.

Note

The card has been designed to use Female 90° Micro-Change to Male straight Micro-Change network cable. The following cable brands are recommended:

- DND32A-M005 (0.5M length)
- DND32A-M010 (1.0M length)
- DND32A-M020 (2.0M length)

2.5.1 Connecting to a DeviceNet Network

DeviceNet network connections for the card are provided through the DeviceNet M12 (Micro) Connector.

2.5.1.1 Termination Resistor

The card does not have a built-in termination resistor. If the card is at the extreme end of the network (end of trunk), connect a 120-ohm termination resistor. This resistor can be inserted along with the DeviceNet cable. Refer to the DeviceNet Specification for more detailed information on termination requirements.

2.5.2 Connecting to a CAN Network

Network connections are made through the DeviceNet M12 (Micro) connector. For more information on the M12, refer to Section 1.4.3.3, Shield.

2.5.2.1 Termination Resistor

The card does not have a built-in termination resistor. You must add termination in accordance with the requirements of the target CAN network.

2.5.2.2 Power

The card requires an external 12-24 VDC power supply. See ODVA DeviceNet Specification Release 2.0, Errata ~ 5 for more details.

2.5.2.3 Grounding

The network shield should be connected directly to earth ground at only one point in the network.

Note

All wiring should be done in accordance with the target CAN Network. The above details are generic and intended only as basic guidelines.

3

Hardware Register Details

Chapter Sections:

- DN3-VME Card Configuration Registers

- Host Register Layout

- Short I/O Registers

3.1 DN3-VME Card Configuration Registers

This chapter provides technical hardware information. The following information is intended for programmers familiar with hardware-level PC programming.

3.2 Host Register Layout

Each channel has its own set of registers, located in short I/O space. The base I/O address is set via the switch. Refer to Section 1.4.5, Dip Switch, for more details.

> **Note**
>
> Upon card power up, or after a physical reset from the system, it typically takes 1 second for the channel to initialize (though it is recommended that applications wait up to 2 seconds). Initialization can be confirmed by monitoring the LEDs or by reading the HDR Register, as described in Section C.1.1, Verifying Card Presence.

Table 16:   Host Register Layout

The following "offsets" are offsets from the base address. A capital "X" means that the bit is reserved (writing to it will result in undefined behavior).

Offset	Register Name	Bit Name							
		7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
01H	Control	CardRun (R/W)	MemEn (R/W)	IntEn (R/W)	WdTout (R)	HostIrq1 (R/W)	HostIrq0 (R/W)	CardIrq1 (R/W)	CardIrq0 (R/W)
03H	AddrMatch (R/W)	AM23	AM22	AM21	AM20	AM19	AM18	AM17	AM16
05H	BankAddress	BA19 (R)	BA18 (R)	BA17 (R/W)	BA16 (R/W)	BA15 (R/W)	BA14 (R/W)	BA13 (R/W)	BA12 (R)
07H	WinSize (R/W)	WS19	WS18	WS17	WS16	WS15	WS14	WS13	WS12
09H	HostIrqID (R/W)	IrqLevel ID							
0BH	LedReg (R)	X	X	PowerRed	PowerGrn	HealthRed	HealthGrn	CommRed	CommGrn
0DH	Debug (R/W)	HWReset	X	X	X	X	X	X	X
0FH	HDR (R)	HostDataReg (written by CPU)							
11H	VMEReg (R/W)	ChID3	ChID2	ChID1	ChID0	X	X	X	SysFail
12H - 1FH		Reserved							

3.3 Short I/O Registers

The card contains the following short I/O registers.

3.3.1 Control Register

This register is a group of control and status bits.

Table 17:   Control Register Settings

Bit	7	6	5	4	3	2	1	0
Name	CardRun	MemEn	IntEn	WdTout	HostIrq1	HostIrq0	CardIrq1	CardIrq0
Read/Write	R/W	R/W	R/W	R	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Each channel has four interrupt flags, two for use in each direction. Setting CardIrq1 or CardIrq0 generates an interrupt to the card with the relevant flag set. When HostIrq1 OR HostIrq0 is '1' and IntEn is '1', the card drives the IRQ pin (as set by the DIP switch).

One flag could be used for a command interface, and another for changing I/O data. The firmware module dictates how these flags are used. If the module uses only one flag, it will be Flag 0.

Note

See Section A.1, USB Port Operation, for details on making the firmware run automatically when the card is booted.

Table 18:   Control Register Bit Descriptions

Bit Name	Description
CardRun	This bit controls and indicates whether or not the card's processor is running. • When this bit is 0, the processor is halted. • When this bit is 1, the processor is running normally. • When this bit is 1, and watchdog has timed out, processor is halted. This bit must remain low for at least 50 µs to guarantee proper reset.
MemEn	High (1) enables shared memory decoding of addresses in this board's range. This board's range is defined by the AddrMatch Register.
IntEn	High (1) enables interrupts on IrqLevel when a HostIrq bit is high (1). • Writing 1 enables interrupts • Writing 0 disables interrupts (the IrqPending flag still functions as described)
WdTout	WdTout high ('1') indicates that a watchdog timeout has occurred, or that the CPU has been held in RESET by some other means. To restore this bit to 0, clear CardRun.
HostIrq1	• This bit is used by the card processor to send interrupts to channel 1 of the host • Writing 1 acknowledges the interrupt and clears it • Writing 0 has no effect • Reading 1 indicates interrupt in progress • Reading 0 indicates interrupt complete
HostIrq0	• This bit is used by the card processor to send interrupts to channel 0 of the host • Writing 1 acknowledges the interrupt and clears it • Writing 0 has no effect • Reading 1 indicates interrupt in progress • Reading 0 indicates interrupt complete
CardIrq1	This bit is used by the host to send interrupts to channel 1 of the card processor • Writing 1 generates an interrupt to the card • Writing 0 has no effect • Reading 1 indicates interrupt in progress • Reading 0 indicates interrupt complete
CardIrq0	This bit is used by the host to send interrupts to channel 0 of the card processor • Writing 1 generates an interrupt to the card • Writing 0 has no effect • Reading 1 indicates interrupt in progress • Reading 0 indicates interrupt complete

3.3.2 AddrMatch Register

This register controls the base memory address of the channel in host memory space.

Each channel may be at a different address. If multiple channels are used at the same address, use MemEn to turn on one channel at a time.

Caution

Setting multiple channels or two cards to the same address and enabling the channels could damage the card permanently.

Table 19:   AddrMatch Register Settings

Bit	7	6	5	4	3	2	1	0
Name	AM23	AM22	AM21	AM20	AM19	AM18	AM17	AM16
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Table 20:   AddrMatch Register Values

Bit and Value								Hex	Address
AM23	AM22	AM21	AM20	AM19	AM18	AM17	AM16		
0	0	0	0	0	0	0	0	0x00	0x000000
0	0	0	0	0	0	0	1	0x01	0x010000
0	0	0	0	0	0	1	0	0x02	0x020000
1	0	1	0	0	1	1	0	0xA6	0xA60000
1	0	1	0	1	0	0	0	0xA8	0xA80000
1	1	1	1	1	1	1	1	0xFF	0xFF0000

Table 21:   AddrMatch Register Bit Descriptions

Bit Name	Description
AM23 – AM16	AM23-AM16 represent the upper address match required to decode memory.
	These bits select the base memory address, from 0x00 to 0xFF0000. For example, writing 0xD0 to this register selects 0xD00000 as the memory base address. Refer to Table 20: AddrMatch Register Values for more details.
	If a 16K window size is selected, AM17-AM16 are ignored and 16K boundaries are used for the memory address. As a result, only even-window boundaries may be chosen. The card could be set to 0xD0000 or 0xD4000 but 0xD2000 would be invalid. Refer to Table 24: WinSize Register Values for information on bit usage with other window sizes.

3.3.3 Bank Address Register

This register is used to switch banks of shared memory into host memory space.

Table 22:   Bank Address Register Values

In this table, the default values are highlighted.

Bit and Value								Window Size and Bank Number					
BA19	BA18	BA17	BA16	BA15	BA14	BA13	BA12	8k	16k	32k	64k	128k	256k
x	x	0	0	0	0	0	x	0	0	0	0	0	0
x	x	0	0	0	0	1	x	1	0	0	0	0	0
x	x	0	0	0	1	0	x	2	1	0	0	0	0
x	x	0	0	0	1	1	x	3	1	0	0	0	0
x	x	0	0	1	0	0	x	4	2	1	0	0	0
x	x	0	0	1	0	1	x	5	2	1	0	0	0
x	x	0	0	1	1	0	x	6	3	1	0	0	0
x	x	0	0	1	1	1	x	7	3	1	0	0	0
x	x	0	1	0	0	0	x	8	4	2	1	0	0
x	x	0	1	0	0	1	x	9	4	2	1	0	0
x	x	0	1	0	1	0	x	10	5	2	1	0	0
x	x	0	1	0	1	1	x	11	5	2	1	0	0
x	x	0	1	1	0	0	x	12	6	3	1	0	0
x	x	0	1	1	0	1	x	13	6	3	1	0	0
x	x	0	1	1	1	0	x	14	7	3	1	0	0
x	x	0	1	1	1	1	x	15	7	3	1	0	0
x	x	1	0	0	0	0	x	16	8	4	2	1	0
x	x	1	0	0	0	1	x	17	8	4	2	1	0
x	x	1	0	0	1	0	x	18	9	4	2	1	0
x	x	1	0	0	1	1	x	19	9	4	2	1	0
x	x	1	0	1	0	0	x	20	10	5	2	1	0

Bit and Value								Window Size and Bank Number					
BA19	BA18	BA17	BA16	BA15	BA14	BA13	BA12	8k	16k	32k	64k	128k	256k
x	x	1	0	1	0	1	x	21	10	5	2	1	0
x	x	1	0	1	1	0	x	22	11	5	2	1	0
x	x	1	0	1	1	1	x	23	11	5	2	1	0
x	x	1	1	0	0	0	x	24	12	6	3	1	0
x	x	1	1	0	0	1	x	25	12	6	3	1	0
x	x	1	1	0	1	0	x	26	13	6	3	1	0
x	x	1	1	0	1	1	x	27	13	6	3	1	0
x	x	1	1	1	0	0	x	28	14	7	3	1	0
x	x	1	1	1	0	1	x	29	14	7	3	1	0
x	x	1	1	1	1	0	x	30	15	7	3	1	0
x	x	1	1	1	1	1	x	31	15	7	3	1	0

* x = don't care

Table 23:   Bank Address Register Bit Descriptions

Bit Name	Description
BA17-13	These bits determine shared addressing sizes and ranges. The power-on state is 0.

3.3.4 WinSize Register

This register controls the window size by masking off the AM19-AM12 and BA19-12 bits in the AddrMatch and Bank Address registers. Table 24, WinSize Register Values, maps the WS bit values required for each valid window size. The default size is 16k.

In this table, the default values are highlighted.

Table 24:   Winsize Register Values

Bit and Value								Window Size	Description
WS19 (R)	WS18 (R)	WS17 (R/W)	WS16 (R/W)	WS15 (R/W)	WS14 (R/W)	WS13 (R/W)	WS12 (R)		
0	0	0	0	0	0	0	1	8K	AM23-AM16 used, BA19-BA13 used, BA12 ignored
0	0	0	0	0	0	1	1	16K	AM23-AM16 used, BA19-BA14 used, BA13-BA12 ignored
0	0	0	0	0	1	1	1	32K	AM23-AM16 used, BA19-BA15 used, BA14-BA12 ignored
0	0	0	0	1	1	1	1	64K	AM23-AM16 used, BA19-BA16 used, BA15-BA12 ignored
0	0	0	1	1	1	1	1	128K	AM23-AM17 used, AM16 ignored BA19-BA17 used, BA16-BA12 ignored
0	0	1	1	1	1	1	1	256K	AM23-AM18 used, AM17-AM16 ignored BA19-BA18 used, BA17-BA12 ignored

Table 25:   WinSize Register Bit Descriptions

Bit Name	Description
WS19-WS12	WS19-WS12 represent the window size, according to Table 24: Winsize Register Values. • Writing any value other than those above has no effect The size of the memory window affects the number of banks required to access all memory. Refer to Table 22: Bank Address Register Values, for more information.

3.3.5 HostIrq ID Register

This register contains an 8-bit IrqLevel ID value written by the host to distinguish the card from other devices that might share the same IRQ level (as set by the DIP switch). This ID is placed on the VME bus during an interrupt acknowledge cycle by the device that generated an IRQ to the host.

3.3.6 LedReg Register

This register reflects the state of card LEDs, allowing host software to monitor the LEDs and display them on-screen.

The LedReg register represents the state of the card LEDs. The state of this register is controlled by the firmware module. Reading the register will reflect the following LED states:

Table 26:   LedReg Register Settings

Bit	7	6	5	4	3	2	1	0
Name	Reserved		PowerRed	PowerGrn	HealthRed	HealthGrn	CommRed	CommGrn
Read/Write	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Table 27:   Power, Comm and Health Status

Bit Name/Value		Description
PowerRed	**PowerGrn**	These bits indicate the state of the card's Power LED
0	0	Invalid
0	1	LED is green
1	0	LED is red
1	1	Invalid
CommRed	**CommGrn**	These bits indicate the state of the card's Comm LED
0	0	LED is off
0	1	LED is green
1	0	LED is red
1	1	LED is amber
HealthRed	**HealthGrn**	These bits indicate the state of the card's Health LED
0	0	LED is off
0	1	LED is green
1	0	LED is red
1	1	LED is amber

3.3.7 Debug Register

This register is reserved for future use.

3.3.8 HDR Register

The HDR register shall be used to pass 1 byte of data from the card to the host. The use of this register is determined by the firmware module/boot code. Refer to the Firmware Reference Guide for details.

3.3.9 VMEReg Register

The VME register is used for VME-specific functions and only contains the VME SysFail bit and ChannelID bits.

The Sysfail LED is directly controlled by the SysFail bit in this register. If this bit is set to a logic '1', the LED will turn red, which indicates a VME system error. It also will assert the VME System failure signal on the backplane.

The following table shows the ChannelID bits. These bits indicate which channel's register set is being read.

Table 28:   ChannelID Bits

Channel	Bit and Value							
	7	6	5	4	3	2	1	0
Channel 1	X	0	0	1	X	X	X	SysFail
Channel 2	X	0	1	0	X	X	X	X
Channel 3	X	0	1	1	X	X	X	X
Channel 4	X	1	0	0	X	X	X	X

4

Troubleshooting

Chapter Sections:

- COMM LED is Red

- Memory Conflict

- General Troubleshooting

For a list of hardware-related errors that can be generated by the card, refer to Section A.2, Card Errors.

⚠️ **Warning**

Only qualified electrical personnel familiar with the construction and operation of this equipment and the hazards involved should install, adjust, operate, or service this equipment. Failure to observe this precaution could result in severe bodily injury or loss of life.

4.1 COMM LED is Red

This section describes strategies for troubleshooting a red COMM LED.

> **Note**
>
> For information on LED flash codes, refer to Section A.2.2,
> Fatal Hardware Self-Test Flash Codes.

If the COMM LED is red, the channel is not running or there has been a firmware run-time error. Check the WdTout bit (refer to Table 18, Control Register Bit Descriptions) to determine whether or not there has been a watchdog timeout, and consult the Firmware Reference Guide if necessary. If you continue to experience difficulties, refer to Section 4.3, General Troubleshooting.

> **Note**
>
> The firmware module must be reloaded to restart the channel.

4.2 Memory Conflict

If a memory conflict is detected, examine the resource allocations in the operating system. If the operating system does not manage resources, review the requirements of the other hardware installed in the machine to select a non-conflicting memory window. If you continue to experience difficulties, refer to Section 4.3, General Troubleshooting.

4.3 General Troubleshooting

If you experience problems with the card:

1. Check the website at http://www.woodhead.com/ for technical notes.

2. Check the FAQs on the website.

3. Refer to Section E.3, Technical Support.

A
Boot Code Operation

Appendix Sections:

- USB Port Operation

- Card Errors

A.1 USB Port Operation

The following sections describe the USB port's operation.

A.1.1 Plugging in the USB Port

To plug in the USB port, follow these steps:

1. Plug one end of the cable into the card. The required cable is USB A-B Cable, male to male. Your PC's operating system automatically detects each channel (USB device) on the card.

2. Plug the remaining end of the cable into the USB port. A generic USB hub and 1, 2 or 4 USB devices will be detected, depending on the number of channels.

A.1.2 Installing the USB Drivers

For details on installing USB drivers, refer to Section 1.4.1, USB Port.

A.1.3 Using the USB BIOS Utility

The BIOS Utility allows you to update firmware and FPGA files, as well as to set manual or autorun modes for firmware operation.

To use the BIOS Utility, follow these steps:

1. On the installation CD, locate the SST Generation 3 BIOS utility and double-click it. The SST Generation 3 BIOS Utility dialog is displayed.

    Figure 7:   SST Generation 3 BIOS Utility Dialog
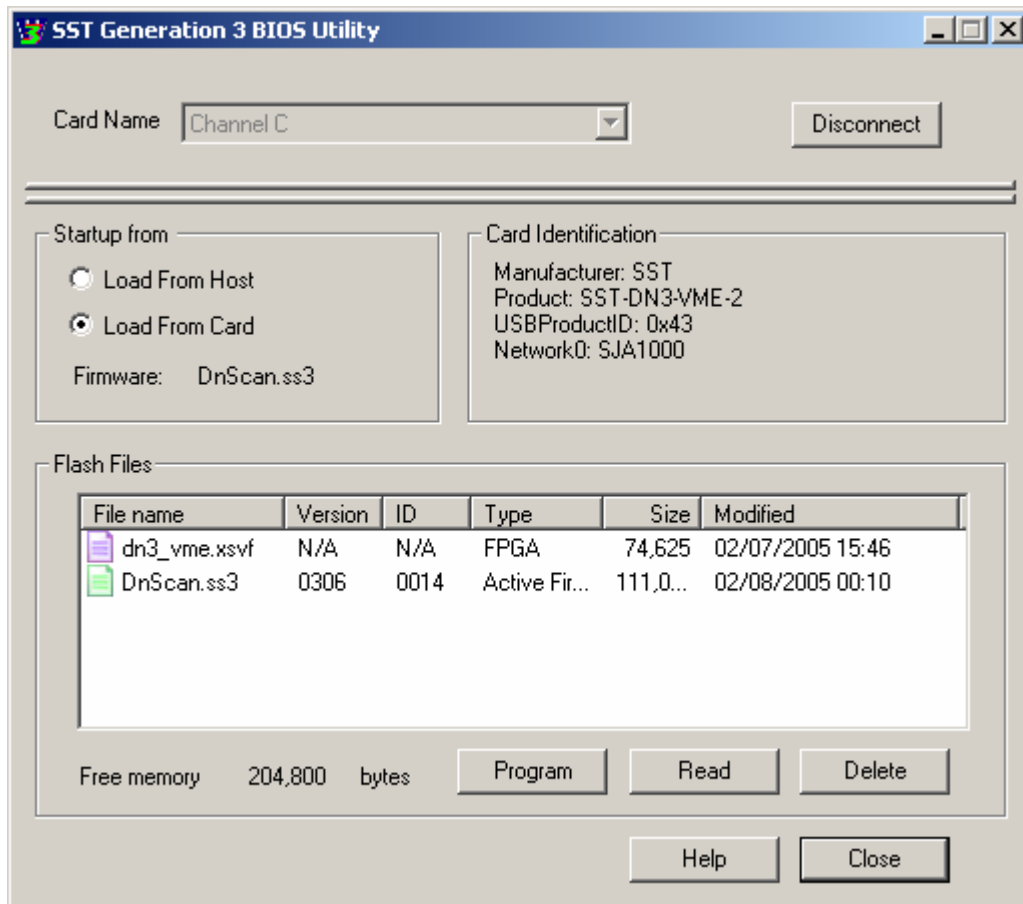
2. Click **Connect** (or **Disconnect**, if the card is already plugged in).

3. Configure your settings as desired. The following table describes the BIOS Utility's options and areas.

Table 29:   USB Utility Options/Areas

Option or Area	Description
Card Name	Corresponds to the channel on the card. Allows you to choose the channel you want to connect to.
Connect/Disconnect	Allows you to toggle between connecting and disconnecting the card.
Startup From	Allows you to choose whether to load the firmware from the Card or from the Host.
Card Identification	Displays the card's ID details.
Flash Files	Lists the available flash files. To select a file, right-click on it.
Program	Allows you to load files into flash.
Read	Allows you to fetch files from flash to host.
Delete	Allows you to delete flash files.

4. Click **Close**.

You can set the BIOS utility to autorun on startup from the card or from the host. To run from the card, select the **Load from Card** radio button. The utility will choose the first available .ss3 file. If you want to use a different .ss3 file, double-click on the desired one.

If autorun is enabled for any channel, there is a 30-second timeout if the USB cable is plugged in before card startup, and no timeout if the cable is not plugged in. If you want to configure a channel that has autorun enabled, the cable must be plugged in before the card is powered up.

If the XSVF file has been deleted and the card is rebooted, the boot code will still allow a USB connection to the BIOS utility, but the LEDs will not function until a valid XSVF file is present on the card.

A.2 Card Errors

The following errors may be reported during the card's startup self-test.

A.2.1 HDR Messages

If HDR reads anything other than 0x40, the card has not been found. To fix the problem, follow these steps:

1. Double-check the switch settings and make sure they match up with the I/O driver port address setting in the software application. For more information on switch settings, refer to Section 1.4.5, DIP Switch.

2. Make sure you have waited up to 2 seconds after the channel reset has been negated before trying to access it.

3. Check for an I/O conflict.

4. If you continue to experience difficulties, refer to Section 4.3, General Troubleshooting.

Note

The default value for boot code is 0x40, but this can be changed by the firmware module. Refer to the Firmware Reference Guide for more details.

For more information on HDR, refer to Table 16, Host Register Layout, and Section 3.3.8, HDR Register.

A.2.2 Fatal Hardware Self-Test Flash Codes

Fatal failures during startup are accompanied by an 8-bit fault code, flashed on the COMM LED. The fault code will be output MSB first, with a 1 (one) bit shown as a green LED, and a zero (0) bit shown as a red LED. This will occur for a period of 900ms, followed by 100ms of off time. The LSB will be followed by an additional 1000ms of off time, after which the sequence will repeat.

The following table describes each possible fault code. If you see any of these codes, please refer to Section E.3 for Technical Support details.

Table 30:   LED Flash Codes

Binary Value		Hex Value	Name	Description
MSB	LSB			
0000	0001	0x01	BITTEST8	Bit test failure of an 8-bit memory range
0000	0010	0x02	BITTEST16	Bit test failure of a 16-bit memory range
0000	0011	0x03	BITTEST32	Bit test failure of a 32-bit memory range
0000	0100	0x04	ADDRTEST8	Address test failure of an 8-bit memory range
0000	0101	0x05	ADDRTEST16	Address test failure of a 16-bit memory range
0000	0110	0x06	ADDRTEST32	Address test failure of a 32-bit memory range
		0x07-0x09	-	Reserved for future fatal start-up errors
0001	0000	0x10	JTAGFAILED	JTAG download failed
0001	0001	0x11	JTAG_ ERROR_UNKNOWN	JTAG programming error
0001	0010	0x12	JTAG_TDOMISMATCH	JTAG output data failed to match expected pattern
0001	0011	0x13	JTAG_MAXRETRIES	JTAG output data failed to match expected pattern after several attempts
0001	0100	0x14	JTAG_ILLEGALCMD	JTAG programming file contained an unknown/malformed command
0001	0101	0x15	JTAG_ERROR_ILLEGALSTATE	JTAG programming file commanded an illegal TAP state transition
0001	0110	0x16	JTAG_ERROR_DATAOVERFLOW	JTAG programming file contained a shift pattern in excess of MAX_LEN * 8 bits
		0x20-0xFF	-	Reserved for firmware-specific fatal errors

B
Technical Specifications

Appendix Sections

- Technical Specifications

B.1 Technical Specifications

The following tables list the technical specifications for the card.

Table 31:   Environmental Specifications

Ambient Conditions	Storage temp:	-25°C to 70°C
	Operating temp:	0°C to 50°C
	Operating Humidity:	5% to 90% non-condensing
Typical Current Draw		+5V +/- 5% 1-channel card: 600 mA 2-channel card: 1000 mA 4-channel card: 2000 mA
VME Compliance		VMEBus Spec VME64-compliant (Vita 1.1 1997)

Table 32:   Network Specifications

Isolation	1000V
Protocol	DeviceNet/CAN
Data Rate	Data rates up to 500kbps All CAN data rates up to 1Mbps

Table 33:   VME Bus Specifications

Size	Double-height (6U) module Standard memory
Resources	16k x 16-bit window per channel, located on a 64k boundary in VME standard space Short memory 1Kbyte range per channel, located on a 1k boundary determined by the DIP switch settings. Refer to Section 1.4.2.1.

Figure 8:   Card Dimensions (Shown Without Bracket)
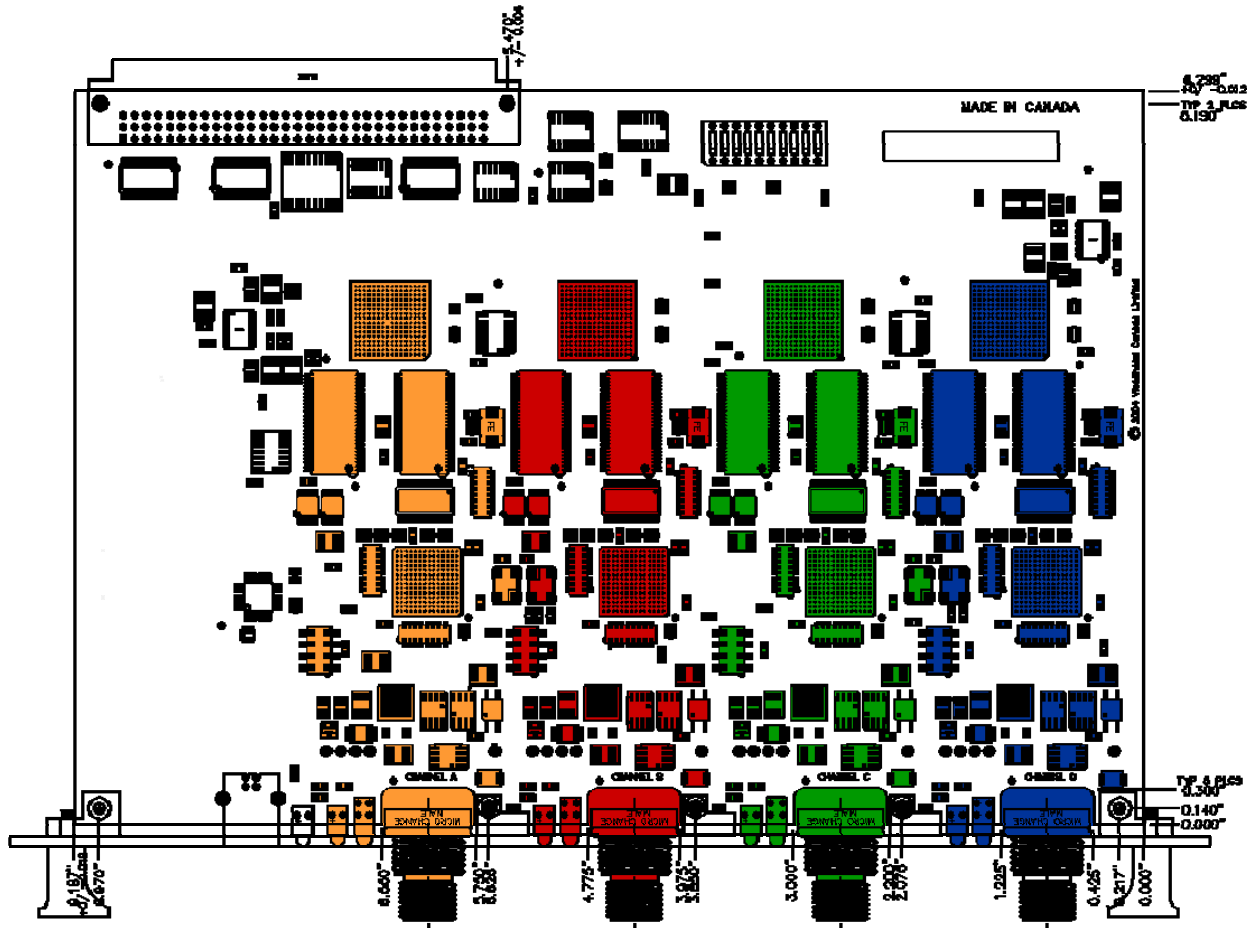
For information on card components, refer to Section 1.4, Hardware Description.

C

Loading a Firmware Module

Appendix Sections:

- Loading a Firmware Module

Note

This appendix describes how to load the card manually, or how to write your own loader.

C.1 Loading a Firmware Module

Firmware modules for the card are supplied as .ss3 files, found on the software CD-ROM and on the website at http://www.woodhead.com/.

If you are developing a driver for the card or producing a stand-alone embedded application, the following section describes the basic sequence of steps to manually load a module onto the card.

Note

For register descriptions, refer to Chapter 3, Hardware Register Details.

C.1.1 Verifying Card Presence

To verify the card's presence, follow these steps:

1. Start up your computer.

2. Following release of the backplane reset, wait at least 1 second (though 2 is recommended).

3. If HDR reads anything other than 0x40, the card is still in Reset or has not been found. Double-check that the Short I/O address matches the DIP Switch setting. If you continue to experience difficulties, contact technical support (refer to Section E.3, Technical Support, for details).

C.1.2 Checking For Conflicting RAM

Before the shared memory on the card can be safely enabled, it must be determined that no other devices in the system are using the intended memory address range.

> **Note**
>
> Any task switching, interrupts or processes should be disabled during this procedure.

To check for conflicting RAM, follow these steps:

1. Write zero (0) to the Control Register to disable the card.

2. Read a word from the target memory window and save it.

3. Write 0xAA55 to the target address.

4. Read the target address. It should not contain 0xAA55.

5. If 0xAA55 is read, a conflict exists. Perform the following steps:

   - Restore the saved value to the target address

   - Abort the load procedure

   - Examine the resource allocations in your operating system. If your operating system does not manage resources, review the requirements of the other hardware installed in your machine to select a non-conflicting memory window. If you continue to experience difficulties, contact technical support (refer to Section E.3, Technical Support, for details).

> **Note**
>
> If you are unsure of the system's memory usage, you may want to do a full memory window verification to ensure that there are no memory conflicts.

C.1.3 Test Card RAM

To test the card RAM, follow these steps:

1. Write the upper byte of the desired 24-bit base address to the AddrMatch Register.

2. Write the desired window size to the WinSize register (refer to Section 3.3.4, WinSize Register, for details). The default value in the window size is 0x03 (16k).

3. Write 0x40 (MemEn) to the Control Register at offset 1.

4. Fill the shared memory with a test pattern.

5. Repeat steps 3-4 for all memory banks.

6. Verify the test pattern.

C.1.4 Loading and Starting the Firmware Module

To load and start the firmware module, follow these steps:

1. Write the contents of the entire firmware file into shared memory, starting at bank zero (0), offset zero (0).

2. If the application requires interrupts from the card, write the interrupt ID to the IrqID Register and bit-wise OR the value 0x20 (IntEn) to the Control Register.

3. Bit-wise OR the value 0x80 (CardRun) to the Control Register to start the firmware module.

4. Start a 2-second timeout timer and wait for bit 2 (HostIrq0) in the Control Register to set.

5. If the timer expires, the firmware module failed to start. Write zero to the Control Register to disable the card. If this problem persists, contact technical support for assistance.

6. Check the load status, as per the Firmware Reference Guide.

D
CE Compliance

Appendix Sections:

- CE Compliance

D.1 CE Compliance

This device meets or exceeds the requirements of the following standard:

- EN 61326:1998 including amendments A1 and A2: - "Electrical equipment for measurement, control and laboratory use - EMC requirements.

⚠️ Warning

This is a Class A product. In a domestic environment this product may cause radio interference in which case you may be required to take adequate measures.

⚠️ Caution

This equipment is neither designed for, nor intended for operation in installations where it is subject to hazardous voltages and hazardous currents.

Marking of this equipment with the symbol $C\!\in$ indicates compliance with European Council Directive 89/336/EEC - The EMC Directive as amended by 92/31/EEC and 93/68/EEC.

📝 Note

To maintain compliance with the limits and requirements of the EMC Directive, it is required to use quality interfacing cables and connectors when connecting to this device. Refer to the cable specifications in the Hardware Guide for selection of cable types.

📝 Note

The backplane voltage supply for this equipment must be delivered as Separated Extra Low Voltage (SELV).

E

Warranty and Support

Appendix Sections:

- Warranty

- Reference Documents

- Technical Support

E.1 Warranty

For warranty information pertaining to the card, refer to http://www.mysst.com/warranty.asp.

E.2 Reference Documents

ODVA DeviceNet Specification Release 2.0, Errata ~ 5
http://www.odva.org/

Vita 1.1 1997
VMEbus International Trade Association

E.3 Technical Support

Please ensure that you have the following information readily available before calling for technical support:

- Card type and serial number

- Computer's make, model and hardware configuration (other cards installed)

- Operating system type and version

- Details of the problem you are experiencing: firmware module type and version, target network and circumstances that may have caused the problem

E.3.1 Getting Help

Technical support is available during regular business hours by telephone, fax or email from any Woodhead Software & Electronics office, or from http://www.woodhead.com/. Documentation and software updates are also available on the website.

📝 **Note**

> If you are using the card with a third-party application, refer to the documentation for that package for information on configuring the software for the card.

North America

Canada:
Tel: 1-519-725-5136
Fax: 1-519-725-1515
Email: techsupportna@woodhead.com

Europe

France:
Tel: 33-(0)2-32-96-04-22
Fax: 33-(0)2-32-96-04-21
Email: supportfr@applicom-int.com

Germany:
Tel: 49-711-782-374-22
Fax: 49-711-782-374-11
Email: supportde@applicom-int.com

Italy:
Tel: 39-01-059-540-52
Fax: 39-0-10-59-56-925
Email: supportit@applicom-int.com

United Kingdom:
Tel: 33-(0)2-32-96-04-23
Fax: 44-161-285-8686
Email: supportintl@applicom-int.com

Asia-Pacific

Japan:
Tel: 81-452-24-3560
Fax: 81-52-745-7622
Email: techsupport@woodhead.co.jp

Singapore:
Tel: 65-64-67-96-52
Fax: 65-6261-3588
Email: info@woodhead.com.sg

China:
Tel: 86-21-5032-8080
Fax: 86-21-5031-8833
Email: techsupport@woodhead.co.jp

For the most current contact details, please visit http://www.woodhead.com/.

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