

# Freescale Semiconductor Addendum

MC9S08AC60AD Rev. 0, 11/2009

## MC9S08AC60 Data Sheet Errata

by: Microcontroller Solutions Group

This errata document describes corrections to the *MC9S08AC60 Series Data Sheet*, order number 1 MC9S08AC60. For convenience, the addenda items are 2 grouped by revision. Please check our website at http://www.freescale.com for the latest updates.

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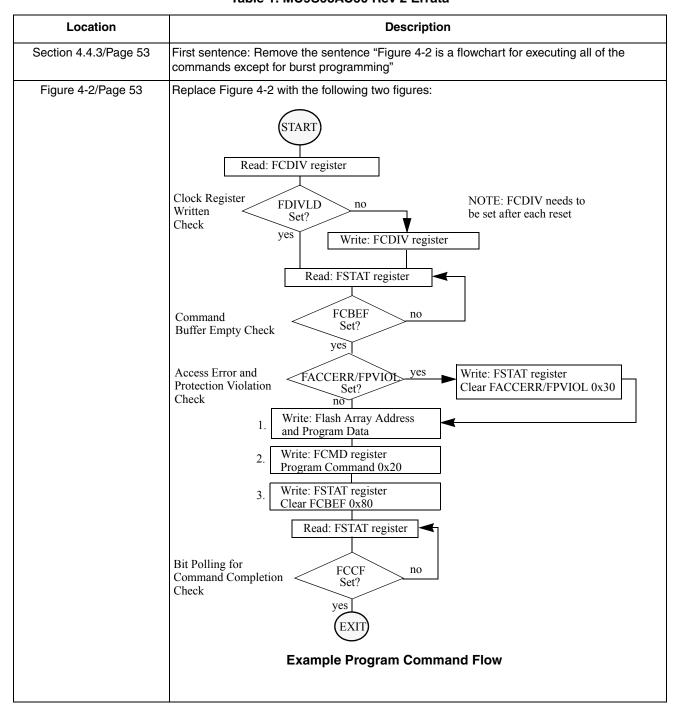
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### 1 Errata for Revision 2

Table 1. MC9S08AC60 Rev 2 Errata





Location Description Read: FCDIV register Clock Register NOTE: FCDIV needs to **FDIVLD** Written be set after each reset Set? Check yes Write: FCDIV register Read: FSTAT register **FCBEF** no Command Set? **Buffer Empty Check** yes Access Error and FACCERR/FPV101\_yes Write: FSTAT register Protection Violation Clear FACCERR/FPVIOL 0x30 Set? Check no Write: Flash Block Address and Dummy Data Write: FCMD register 2. Erase Verify Command 0x05 Write: FSTAT register 3. Clear FCBEF 0x80 Read: FSTAT register Bit Polling for **FCCF** no **Command Completion** Set? Check yes Erase Verify FBLANK Status Set? yes Flash Block Flash Block EXI Erased Not Erased **Example Erase Verify Command Flow** Section 4.4.6/Page 55 First paragraph, fourth sentence: change from "...3-bit control field..." to "... 7-bit control field..." Remove the sentence "A separate control bit allows block protection of the entire FLASH memory array". Last sentence: change from "All seven of these control bits..." to "All eight of these control

Table 1. MC9S08AC60 Rev 2 Errata (continued)

bits.."



Table 1. MC9S08AC60 Rev 2 Errata (continued)

Location		Description					
Table 15-8/Page 268	Replace Table 15-8 with the following table to show "Software compare only" configuration for the "Output compare" mode.						
	Mode, Edge, and Level Selection						
	CPWMS	MSnB:MSnA	ELSnB:ELSnA	Mode	Configuration		
	Х	XX	00	Pin is not controlled by TPM. It is reverted to general purpose I/O or other peripheral control			
	0	00	01	Input capture	Capture on rising edge only		
			10		Capture on falling edge only		
			11		Capture on rising or falling edge		
		01	00	Output compare	Software compare only		
			01		Toggle output on channel match		
			10		Clear output on channel match		
			11		Set output on channel match		
		1X	10	Edge-aligned PWM	High-true pulses (clear output on channel match)		
			X1		Low-true pulses (set output on channel match)		
	1	xx	10	Center-aligned PWM	High-true pulses (clear output on channel match when TPM counter is counting up)		
			X1		Low-true pulses (set output on channel match when TPM counter is counting up)		

### 2 Revision History

Table 2 provides a revision history for this document.

Table 2. MC9S08AC60AD Revision History

Rev. Number	Substantive Changes	Date of Release
0	Initial release	11/2009



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