UM11137

QN9080-001-M17 User Manual

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Document information

Info	Content
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Abstract	QN9080-001-M17 user manual

Revision history

Rev	Date	Description
1.0	12/2018	Public release

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1. About This Book

This manual details the QN9080-001-M17, which is system-in-package (SIP) device that comprises of QN9080, NTAG and bluetooth antenna parts.

1.1 Audience

This manual is intended for system designers.

1.2 Related documents

This book provides only the overall information about this QN9080-001-M17. Refer to the following documents for details of each parts. You can use the Document ID or Document Number to search and find those books at nxp.com.

Table 1. Related documents

Related doc	Document ID	Document Number
QN908x user manual	UM11023	—
NT3H2111_2211 Product Data Sheet	NT3H2111_2211	359932

2. Compliance statements and documentation

- The FCC ID number of the QN9080-001-M17 is XXMQN9080M17
- The IC ID number of the QN9080-001-M17 is 8764A-QN9080M17
- The Japan ID number of the QN9080-001-M17 is 207-990010

2.1 FCC Statements and documentation

This section contains the Federal Communication Commission (FCC) statements and documents.

2.1.1 FCC interference Statements

- This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one of the following measures:
  - Reorient or relocate the receiving antenna
  - Increase the separation between the equipment and receiver
  - Connect the equipment into an outlet on a circuit different from that to which the receiver is connected
  - Consult the dealer or an experienced radio/TV technician for help
- OEM integrators instructions

- The OEM integrators are responsible for ensuring that the end-user has no manual instructions to remove or install SIP
- The SIP is limited to installation in mobile or fixed applications, according to CFR 47 Part 2.1091(b)
- Separate approval is required for all other operating configurations, including portable configurations with respect to CFR 47 Part 2.1093 and different antenna configurations

- User guide mandatory statements

  User's instructions of the host device must contain the following statements in addition to operation instructions:

  * "This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions:

  (1) This device may not cause harmful interference, and

  (2) This device must accept any interference received, including interference that may cause undesired operation"

  * "Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment"

- FCC RF Exposure requirements

  User's instructions of the host device must contain the following instructions in addition to operation instructions:

  Avoid direct contact to the antenna, or keep it to a 20cm minimum distance while using this equipment. This device must not be collocated or operating in conjunction with another antenna or transmitter.

This SIP has been designed to operate etheir with internal antenna or with external antennas having a maximum gain of 2 dBi. Antennas having a gain greater than 2 dBi are strictly prohibited for use with this device. The required antenna impedance is 50 ohms

2.1.2 FCC end product labelling

The final 'end product' should be labelled in a visible area with the following:
"Contains TX FCC ID: XXMQN9080M17 to reflect the SIP being used inside the product.

2.2 Industry Canada Statement

This device complies with Industry Canada licence-exempt RSS standard(s). Operation is subject to the following two conditions: (1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device. This device complies with Industry Canada RF radiation exposure limits set forth for general population (uncontrolled exposure). This device must be installed to provide a separation distance of at least 20 cm from all persons and must not be collocated or operating in conjunction with any other antenna or transmitter.	Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes : (1) il ne doit pas produire de brouillage, et (2) l'utilisateur du dispositif doit être prêt à accepter tout brouillage radioélectrique re?u, même si ce brouillage est susceptible de compromettre le fonctionnement du dispositif. Le présent appareil est conforme aux niveaux limites d'exigences d'exposition RF aux personnes définies par Industrie Canada. Cet appareil doit être installé afin d'offrir une distance de séparation d'au moins 20 cm avec l'utilisateur, et ne doit pas être installé à proximité ou être utilisé en conjonction avec une autre antenne ou un autre émetteur.

To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropic radiated power (e.i.r.p.) is not more than that permitted for successful communication.

The Gain of SIP with internal antenna is -3dBi.

If customer wants, he can also use the SIP with external antenna with maximum gain of 2dbi. This feature is not certified by NXP and need to be done by the customer. Antennas having a gain greater than 2 dBi are strictly prohibited for use with this device. The required antenna impedance is 50 ohms.

As long as the above condition is met, further transmitter testing will not be required.

However, the OEM integrator is still responsible for testing their end-product for any additional compliance requirements required with this SIP installed (for example, digital device emissions, PC peripheral requirements, etc.).

2.2.1 Industry of Canada end product labelling

For Industry Canada purposes the following should be used:
"Contains Industry Canada ID IC: 8764A-QN9080M17

2.3 Japanese Radio Certification Statement

This equipment has been tested and found to comply with the Japanese Radio Certification Rules

2.3.1 Radio Certification end product labelling

For Japanese Radio Certification purposes, the following should be used:

"Contains Japanese Radio certificate product: Japan ID number is 207-990010

3. QN9080-001-M17 Introduction and Chip Configuration

3.1 General description

The QN9080-001-M17 is a fully certified device supporting BLE and NFC. It has ultra-low power consumption, highly integrated with rich feature sets, fully FCC/CE/IC/MIC certified. The QN9080-001-M17 supports Bluetooth 5, and it is intended for ultra-small, portable connected wireless applications.

This ultra-small device is based on QN9080 die and NT3H2211 die. QN9080 is powered by an Arm® Cortex®-M4F, and has a dedicated fusion sensor co-processor (FSP) to further reduce power consumption by off-loading complex math computations to the hardware. 512 KB of on-board flash and 128 KB SRAM provide enough room and flexibility for complex applications. NT3H2211 is NFC Forum Type 2 Tag compliant IC with I^2C interface, which supplies the fastest, least expensive way to add tap-and-go connectivity to just about any electronic applications.

The QN9080-001-M17 also integrates 32 MHz and 32.768 kHz crystals, a 2.4 GHz optimized antenna and necessary components for QN9080 system to run. It offers a complete solution for applications requiring BLE wireless connectivity and fast pairing with NTAG as an option. Its low external component count reduces overall system size, complexity and shortens development time.

3.2 Block diagram

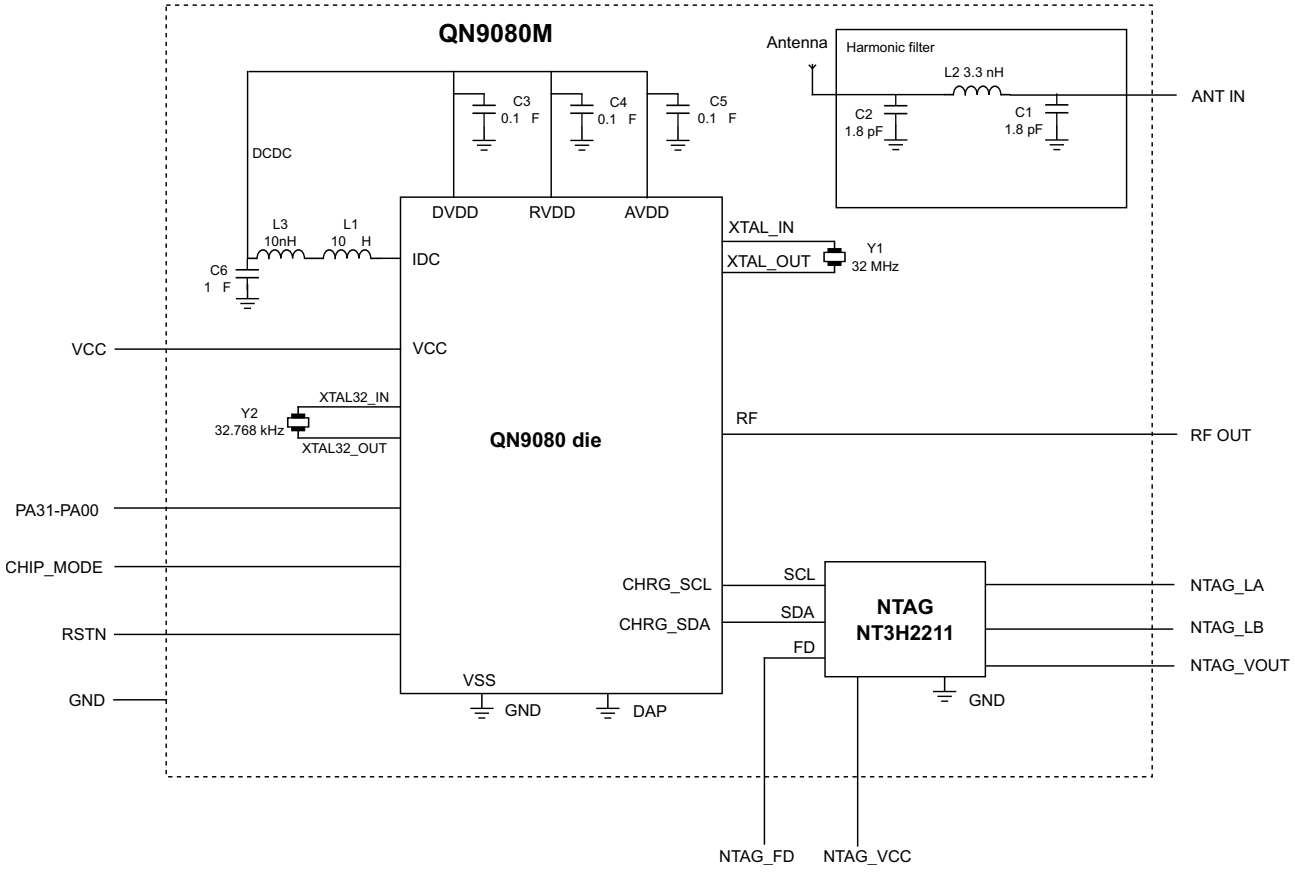

Fig 1. QN9080-001-M17 – high level HW block diagram

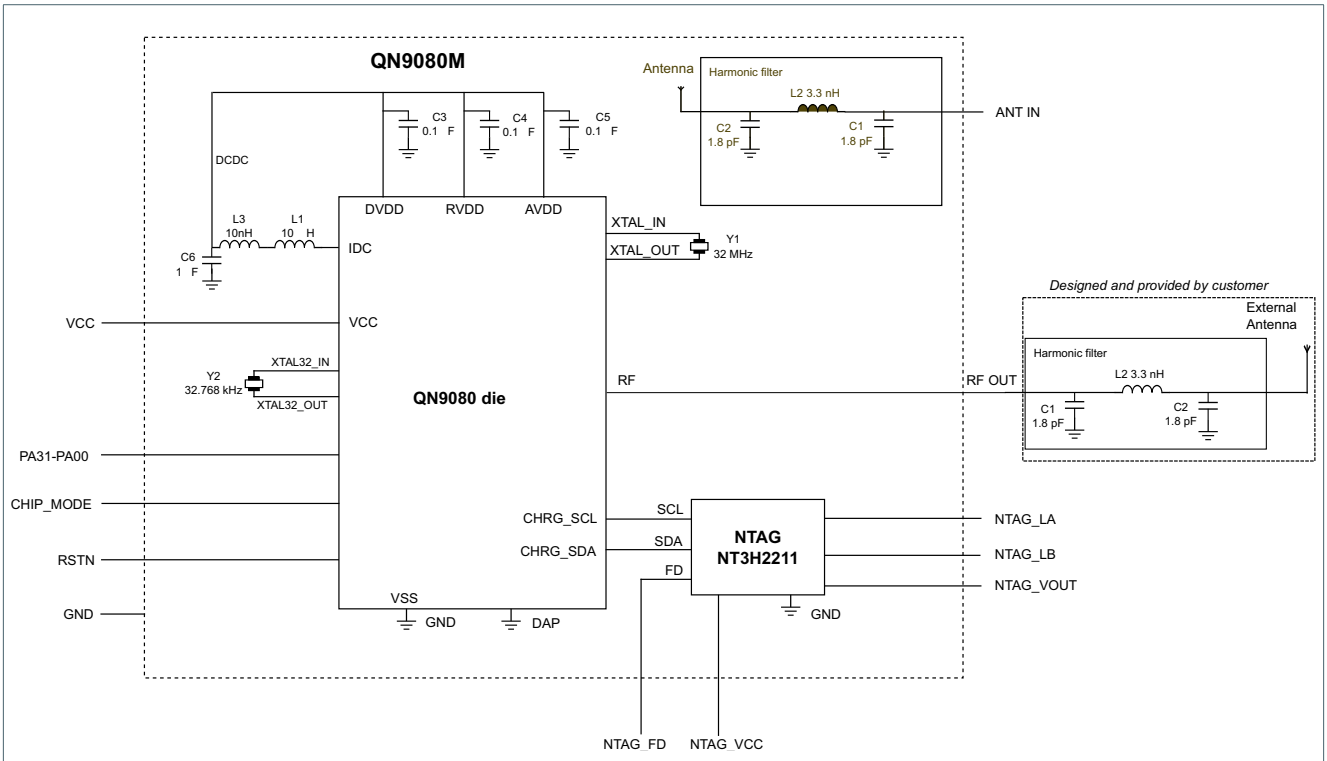

Fig 2. QN9080-001-M17 block diagram using external antenna

Remark: (1) QN9080-001-M17 is not certified with external antenna but only with its internal antenna. Customer using external antenna will have to do new certification. (2) Harmonic filter is in adequacy with board.

3.3 Features and benefits

- Key features:
  - Bluetooth 5.0 certified
  - Integrated antenna
  - Integrated 32 MHz and 32.768 kHz crystals
  - 32-bit Arm Cortex-M4F core at 32 MHz
  - 512 KB flash
  - 128 KB RAM
  - TX power: up to +2 dBm
  - RX sensitivity: -92.7 dBm in 1 Mbps mode and -89 dBm in 2 Mbps mode
- True single-chip Bluetooth Low Energy (v5.0) SoC solution
  - Integrated Bluetooth LE radio, protocol stack and application profiles
  - Support central and peripherals roles
  - Support master/slave concurrency
  - Support 16 simultaneous links

  - Support secure connections
  - Support data packet length extension
  - 48-bit unique BD address
  - -92.7 dBm in 1 Mbps mode and -89 dBm in 2 Mbps mode
  - TX output power from -20 dBm to +2 dBm
- Very low power consumption
  - Single 1.67 V ~3.6 V power supply
  - 1 μA power-down mode, to wake up by GPIO
  - 2 μA power-down mode, to wake up by 32 kHz sleep timer, RTC and GPIO
  - 4 mA RX current at 3 V supply in 1 Mbps mode
  - 3.5 mA TX current at 0 dBm TX power at 3 V in 1 Mbps mode
- Interface
  - 32 General-Purpose Input/Output (GPIO) pins, with configurable pull-up/pull-down resistors
  - 8 external ADC inputs (shared with GPIO pins)
  - 2 Analog Comparator input pins (shared with GPIO pins)
- Single power supply 1.67 V to 3.6 V
- Operating temperature range: -40 °C to +85 °C
- 6 x 9.7 x 1.17 mm LFLGA package

3.3.1 Feature of QN9080

- True single-chip Bluetooth Low Energy (v5.0) SoC solution
  - Integrated Bluetooth LE radio, protocol stack and application profiles
  - Supports central and peripherals roles
  - Supports master/slave concurrency
  - Supports 16 simultaneous links
  - Supports secure connections
  - Supports data packet length extension
  - Wifi/Bluetooth LE coexistence interface
  - 48-bit unique bluetooth device address
- RF
  - Fast and reliable RSSI in 1dB step
  - TX output power from -20 dBm to 2 dBm
  - Single-ended RF port with integrated balun
  - Generic FSK modulation with programmed data rate from 250 KB/s to 2 MB/s
  - Compatible with worldwide radio frequency regulations
- Very low power consumption
  - Single 1.67 V to 3.6 V power supply
  - Integrated DC-to-DC buck converter and LDO

  - 1.0 μA power-down 1 mode, to wake up by GPIO
  - 2.5 μA power-down 0 mode, to wake up by 32 kHz sleep timer, RTC and GPIO
  - 3.5 mA RX current with DC-to-DC convertor enabled at 3 V supply in 1 Mbps mode
  - 4 mA TX current at 0 dBm TX power with DC-to-DC converter enabled at 3 V supply in 1 Mbps mode
- Arm Cortex-M4 core (version r0p1)
  - Arm Cortex-M4 processor, running at a frequency of up to 32 MHz
  - Floating Point Unit (FPU) and Memory Protection Unit (MPU)
  - Arm Cortex-M4 built-in Nested Vectored Interrupt Controller (NVIC)
  - Serial Wire Debug (SWD) with six instruction breakpoints, two literal comparators, and four watch points, including serial wire output for enhanced debug capabilities
  - System tick timer
- On-chip memory
  - 512 KB on-chip flash program memory and 2 KB page erase and write
  - 128 KB SRAM
  - 256 KB ROM
- ROM API support
  - Flash In-System Programming (ISP)
- Serial interfaces
  - Four Flexcomm serial peripherals
  - USART protocol supported by Flexcomm0, USART and I^2C by Flexcomm1, SPI and I^2C by Flexcomm2, and SPI by Flexcomm3
  - Each Flexcomm includes a FIFO
  - I^2C-bus interfaces support fast mode and with multiple address recognition and monitor mode
  - USB 2.0 (full speed) device interface
  - Two quadrature decoders
  - SPI Flash Interface (SPIFI) uses a SPI bus superset with four data lines to access off-chip quad SPI flash memory at a much higher rate than is possible using standard SPI or SSP interfaces
  - Supports SPI memories with 1 or 4 data lines
- Digital peripherals
  - DMA controller with 20 channels, able to access memories and DMA capable peripherals
  - Up to 35 General Purpose Input Output (GPIO) pins, with configurable pull-up or pull-down resistors
  - GPIO registers are located on the AHB for fast access
  - 32 GPIOs can be selected as Pin INTerrupts (PINT), triggered by rising, or falling input edges
  - AES-128 security coprocessor
  - Random Number Generator (RNG)

  - CRC engine
  - Fusion Signal Processor (FSP) for data fusion and machine learning algorithms resulting in low power consumption compared to software processing
- Analog peripherals
  - 16-bit ADC with 8 external input channels, with sample rates of up to 32k sample per second, and with multiple internal and external trigger inputs
  - Integrated temperature sensor, connected to one internal dedicated ADC channel
  - Integrated battery monitor connected to one internal dedicated ADC channel
  - General-purpose 8-bit 1M sample per second DAC
  - Integrated capacitive sense up to 8 channels, able to wake up the MCU from low power states.
  - Two ultra low-power analog comparators, able to wake up the MCU from low power states.
- Timers
  - Four 32-bit general-purpose timers or counters, support capture inputs and compare outputs, PWM mode, and external count input
  - Sleep timer, which can work in power-down mode and wake up MCU
  - 32-bit Real Time Clock (RTC) with 1 second resolution running in the always-on power domain; can be used for wake-up from all low power modes including power-down
  - Watchdog Timer.
  - SC Timer or PWM.
- Clock generation
  - 32 MHz internal RC oscillator, which can be used as a system clock
  - 16 MHz or 32 MHz crystal oscillator, which can be used as a system and RF reference
  - 32 kHz on-chip RC oscillator
  - 32.768 kHz crystal oscillator
- Power control
  - Programmable Power Management Unit (PMU) to minimize power consumption
  - Reduced power modes: sleep, and power-down
  - Power-On Reset (POR)
  - Brown-Out Detection (BOD) with separate thresholds for interrupt and forced reset
- Single power supply 1.67 V to 3.6 V
- Operating temperature range -40 °C to +85 °C

3.3.2 Features of NTAG

- Interoperability
  - ISO/IEC 14443 Part 2 and 3 compliant
  - NTAG I^2C plus development board is certified as NFC Forum Type 2 Tag (Certification ID: 58514)

- Unique 7-byte UID
- GET_VERSION command for easy identification of chip type and supported features
- Input capacitance of 50 pF

- Host interface
  - I^2C slave
  - Configurable event detection pin to signal NFC or pass-through data events
- Memory
  - 1912 bytes of EEPROM-based user memory
  - 64 bytes SRAM buffer for transfer of data between NFC and I^2C interfaces with memory mirror or pass-through mode
  - Clear arbitration between NFC and I^2C memory access
- Data transfer
  - Pass-through mode with 64-byte SRAM buffer
  - FAST_WRITE and FAST_READ NFC commands for higher data throughput
- Security and memory-access management
  - Full, read-only, or no memory access from NFC interface, based on 32-bit password
  - Full, read-only, or no memory access from I^2C interface
  - NFC silence feature to disable the NFC interface
  - Originality signature based on Elliptic Curve Cryptography (ECC) for simple, genuine authentication
- Power management
  - Configurable field-detection output signal for data-transfer synchronization and device wake-up
  - Energy harvesting from NFC field, so as to power external devices (e.g. connected microcontroller)

3.3.3 Features of integrated 2.4 GHz antenna

- Monolithic SMD with small, low-profile and light-weight type.
- Wide bandwidth
- RoHS compliant

Remark: When NFC function is required, the NFC tag antenna needs to be connected externally.

4. Pins and Connections

4.1 Device pin assignment

The following figure shows QN9080-001-M17 pin assignments.

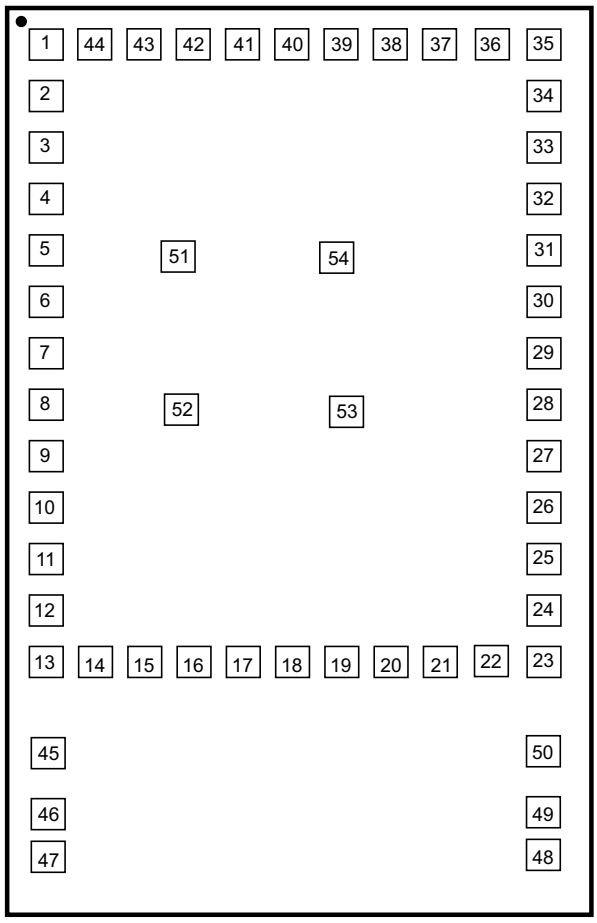

Fig 3. QN9080-001-M17 pinout diagram

4.2 Pin descriptions

Table 2. Pin description

Symbol	LFLGA54	Reset state[1]	Alternate function	Type	Description
PA30	1	PU	GPIOA30	I/O	general-purpose digital input-output pin
			ACMP1P	AI	analog comparator 1 positive input
			ETM_TRACEDAT3	O	ETM trace data output bit 3
			CTIMER3_MAT1	O	timer 3 match output 1
			FC2_SCK	I/O	flexcomm 2: SPI clock
			FC3_MOSI	I/O	flexcomm 3: SPI MOSI
			SPIFI_IO3	I/O	data bit 3 for the SPI flash interface
PA29	2	PU	GPIOA29	I/O	general-purpose digital input-output pin
			ACMP1N	AI	analog comparator 1 negative input
			ETM_TRACEDAT2	O	ETM trace data output bit 2
			CTIMER3_MAT0	O	timer 3 match output 0
			FC2_SCK	I/O	flexcomm 2: SPI clock
			FC3_MISO	I/O	flexcomm 3: SPI MISO
			SPIFI_IO2	I/O	data bit 2 for the SPI flash interface
PA28	3	PU	GPIOA28	I/O	general-purpose digital input output pin
			CLK_AHB	O	AHB clock output
			ETM_TRACECLK	O	ETM trace clock output
			RTC_CAP	I	RTC capture input
			FC1_SCK	I/O	flexcomm 1: USART clock
			SD_DAC	O	sigma-delta modulator DAC output
			SPIFI_CSN	O	active low chip select output for the SPI flash interface
PA27	4	PU	GPIOA27	I/O	general-purpose digital input output pin
			USB_DM	I/O	USB0 bidirectional D- line
			SCT0_IN1	I	SCTimer input 1
			CTIMER1_MAT2	O	32-bit CTimer 1 match output 2
			FC2_SCL_MISO	I/O	flexcomm 2: I^2C SCL, SPI MISO
			QDEC0_B	I	quadrature decoder 0 input channel B
			BLE_IN_PROC	O	BLE event in process indicator for coexistence
PA26	5	PU	GPIOA26	I/O	general-purpose digital input output pin
			USB_DP	I/O	USB0 bidirectional D+ line
			SCT0_IN0	I	SCTimer input 0
			CTIMER1_MAT0	O	32-bit CTimer 1 match output 0
			FC2_SDA_MOSI	I/O	flexcomm 2: I^2C SDA, SPI MOSI
			QDEC0_A	I	quadrature decoder 0 input channel A
			BLE_SYNC	O	BLE sync pulse
LB	6	—	—	RF	NTAG antenna/coil terminal B
LA	7	—	—	RF	NTAG antenna/coil terminal A

Table 2. Pin description *…continued*

Symbol	LFLGA54	Reset state[1]	Alternate function	Type	Description
PA25	8	PU	GPIOA25	I/O	general-purpose digital input-output pin
			ACMP0P/CS7	AI	analog comparator 0 positive input, or capacitive touch sense button input 7
			ETM_TRACEDAT1	O	ETM trace data output bit 1
			CTIMER3_CAP1	I	timer 3 input capture 1
			RFE_TX_EN	O	TX enable for external RF front-end
			FC3_SSEL0	I/O	flexcomm 3: SPI SSEL0
			SPIFI_IO1	I/O	data bit 1 for the SPI flash interface
PA24	9	PU	GPIOA24	I/O	general-purpose digital input output pin
			ACMP0N/CS6	AI	analog comparator 0 negative input, or capacitive touch sense button input 6
			ETM_TRACEDAT0	O	ETM trace data output bit 0
			CTIMER3_CAP0	I	timer 3 input capture 0
			RFE_RX_EN	O	RX enable for external RF front-end
			FC3_SSEL1	I/O	flexcomm 3: SPI SSEL1
			SPIFI_IO0	I/O	data bit 0 for the SPI flash interface
SWDIO/ PA23	10	PU	SWDIO	I/O	serial wire debug I/O; it is the default function after booting
			GPIOA23	I/O	general-purpose digital input output pin
			SCT0_IN3	I	SCTimer input 3
			CTIMER3_MAT1	O	32-bit CTimer 3 match output 1
			FC2_SCL_SSEL1	I/O	flexcomm 2: I^2C SCL, SPI SSEL1
			FC3_SSEL2	I/O	flexcomm 3: SPI SSEL2
			QDEC1_B	I	quadrature decoder 1 input channel B
SWCLK /PA22	11	PU	SWCLK	I/O	serial wire clock; it is the default function after reset
			GPIOA22	I/O	general-purpose digital input output pin
			SCT0_IN2	I	SCTimer input 2
			CTIMER3_MAT0	O	32-bit CTimer 3 match output 0
			FC2_SDA_SSEL0	I/O	flexcomm 2: I^2C SDA, SPI SSEL0
			FC3_SSEL3	I/O	flexcomm 3: SPI SSEL3
			QDEC1_A	I	quadrature decoder 1 input channel A
PA21	12	PU	GPIOA21	I/O	general-purpose digital input output pin
			QDEC1_B	I	quadrature decoder 1 input channel B
			SCT0_OUT0	O	SCTimer output 0, PWM output 0
			CTIMER2_MAT1	O	32-bit CTimer 2 match output 1
			FC2_SSEL3	I/O	flexcomm 2: SPI SSEL3
			FC1_CTS_SDA	I/O	flexcomm 1: USART CTS, I2C SDA
			SPIFI_CSN	O	active low chip select output for the SPI flash interface

Table 2. Pin description *…continued*

Symbol	LFLGA54	Reset state[1]	Alternate function	Type	Description
PA20	13	PU	GPIOA20	I/O	general-purpose digital input output pin
			QDEC1_A	I	quadrature decoder 1 input channel A
			SCT0_OUT1	O	SCTimer output 1, PWM output 1
			CTIMER2_MAT0	O	32-bit CTimer 2 match output 0
			SWO	I/O	serial wire trace output
			FC1_RTS_SCL	I/O	flexcomm 1: USART RTS, I^2C SCL
			SPIFI_CLK	O	clock output for the SPI flash interface
PA19	14	PU	GPIOA19	I/O	general-purpose digital input output pin
			CS5	AI	capacitive touch sense button input 5
			SCT0_OUT2	O	SCTimer output 2, PWM output 2
			RFE_EN	O	enable for external RF front-end
			FC0_SCK	I/O	flexcomm 0: USART clock
			FC3_SSEL3	I/O	flexcomm 3: SPI SSEL3
			BLE_IN_PROC	O	BLE event in process indicator for coexistence
PA18	15	PU	GPIOA18	I/O	general-purpose digital input output pin
			CS4	AI	capacitive touch sense button input 4
			SCT0_OUT3	O	SCTimer output 3, PWM output 3
			CTIMER2_MAT2	O	32-bit CTimer 2 match output 2
			FC0_SCK	I/O	flexcomm 0: USART clock
			FC3_SSEL2	I/O	flexcomm 3: SPI SSEL2
			BLE_SYNC	O	BLE sync pulse
PA17	16	PU	GPIOA17	I/O	general-purpose digital input output pin
			CS3	AI	capacitive touch sense button input 3
			SD_DAC	O	sigma-delta modulator DAC output
			CTIMER2_MAT1	O	32-bit CTimer 2 match output 1
			FC0_RXD	I/O	flexcomm 0: USART RXD
			FC3_MISO	I/O	flexcomm 3: SPI MISO
			QDEC0_B	I	quadrature decoder 0 input channel B
PA16	17	PU	GPIOA16	I/O	general-purpose digital input output pin
			CS2	AI	capacitive touch sense button input 2
			SCT0_OUT1	O	SCTimer output 1, PWM output 1
			CTIMER2_MAT0	O	32-bit CTimer 2 match output 0
			FC0_TXD	I/O	flexcomm 0: USART TXD
			FC3_MOSI	I/O	flexcomm 3: SPI MOSI
			QDEC0_A	I	quadrature decoder 0 input channel A

Table 2. Pin description *…continued*

Symbol	LFLGA54	Reset state[1]	Alternate function	Type	Description
PA15	18	PU	GPIOA15	I/O	general-purpose digital input output pin
			CS1	AI	capacitive touch sense button input 1
			SCT0_OUT0	O	SCTimer output 0, PWM output 0
			CTIMER2_CAP1	I	timer 2 input capture 1
			FC0_CTS	I/O	flexcomm 0: USART CTS
			FC3_SCK	I/O	flexcomm 3: SPI clock
			QDEC1_B	I	quadrature decoder 1 input channel B
PA14	19	PU	GPIOA14	I/O	general-purpose digital input output pin
			CS0	AI	capacitive touch sense button input 0
			ANT_SW	O	external antenna switch for diversity
			CTIMER2_CAP0	I	timer 2 input capture 0
			FC0_RTS	I/O	flexcomm 0: USART RTS
			FC3_SSEL0	I/O	flexcomm 3: SPI SSEL0
			QDEC1_A	I	quadrature decoder 1 input channel A
PA13	20	PU	GPIOA13	I/O	general-purpose digital input output pin
			R	I/O	reserved
			SCT0_OUT4	O	SCTimer output 4
			ACMP1_OUT	O	analog comparator 1 output
			FC1_RXD_SDA	I/O	flexcomm 1: USART RXD, I2C SDA
			FC3_SSEL1	I/O	flexcomm 3: SPI SSEL1
			RFE_EN	O	enable for external RF front-end
CHIP_MODE/PB02	21	PU	CHIP_MODE	I	boot selection with pull-up by default; it should be pulled low to go through the normal ISP process for firmware programming, otherwise the ISP process is escaped to jump to flash
			GPIOB02	I/O	general-purpose digital input output pin
			ANT_SW	O	external antenna switch for diversity
RSTN	22	PU	—	I	active low reset input
ANT_IN	23	—	—	RF	Internal antenna
RF_OUT	24	—	—	RF	RF input output port with Tx or Rx switch integrated on chip
GND	25	—	—		ground
PA12	26	PU	GPIOA12	I/O	general-purpose digital input output pin
			R	O	reserved
			SCT0_OUT5	O	SCTimer output 5
			ACMP0_OUT	O	analog comparator 0 output
			FC1_TXD_SCL	I/O	flexcomm 1: USART TXD, I^2C SCL
			SD_DAC	O	sigma-delta modulator DAC output
			ANT_SW	O	external antenna switch for diversity

Table 2. Pin description *…continued*

Symbol	LFLGA54	Reset state[1]	Alternate function	Type	Description
PA11	27	PU	GPIOA11	I/O	general-purpose digital input output pin
			ADC7	AI	ADC external input 7
			SCT0_IN3	I	SCTimer input 3
			CTIMER1_MAT2	O	32-bit CTimer 1 match output 2
			FC2_SSEL2	I/O	flexcomm 2: SPI SSEL2
			ACMP1_OUT	O	analog comparator 1 output
			BLE_RX	O	BLE reception indicator for coexistence
PA10	28	PU	GPIOA10	I/O	general-purpose digital input output pin
			ADC6	AI	ADC external input 6
			SCT0_IN2	I	SCTimer input 2
			CTIMER1_MAT1	O	32-bit CTimer 1 match output 1
			FC1_SCK	I/O	flexcomm 1: USART clock
			ACMP0_OUT	O	analog comparator 0 output
			BLE_TX	O	BLE transmit indicator for coexistence
PA09	29	PU	GPIOA9	I/O	general-purpose digital input output pin
			ADC5	AI	ADC external input 5
			SCT0_IN1	I	SCTimer input 1
			CTIMER1_MAT0	O	32-bit CTimer 1 match output 0
			FC1_RXD_SDA	I/O	flexcomm 1: USART RXD, I2C SDA
			BLE_PTI3	O	BLE packet traffic information bit 3
			SPIFI_IO3	I/O	data bit 3 for the SPI flash interface
PA08	30	PU	GPIOA8	I/O	general-purpose digital input output pin
			ADC4	AI	ADC external input 4
			SCT0_IN0	I	SCTimer input 0
			CTIMER1_CAP1	I	timer 1 input capture 1
			FC1_TXD_SCL	I/O	flexcomm 1: USART TXD, I2C SCL
			BLE_PTI2	O	BLE packet traffic information 2
			SPIFI_IO2	I/O	data bit 2 for the SPI flash interface
PA07	31	PU	GPIOA7	I/O	general-purpose digital input output pin
			ADC_VREFI	AI	ADC external reference voltage input
			SCT0_OUT2	O	SCTimer output 2
			CTIMER1_CAP0	I	timer 1 input capture 0
			FC1_CTS_SDA	I/O	flexcomm 1: USART CTS, I2C SDA
			BLE_PTI1	O	BLE packet traffic information 1
			SPIFI_CSN	O	active low chip select output for the SPI flash interface

Table 2. Pin description *…continued*

Symbol	LFLGA54	Reset state[1]	Alternate function	Type	Description
PA06	32	PU	GPIOA6	I/O	general-purpose digital input output pin
			ADC_EX_CAP	A	connected with ADC external capacitor
			SCT0_OUT3	O	SCTimer output 3
			CTIMER0_MAT2	O	32-bit CTimer 0 match output 2
			FC1_RTS_SCL	I/O	flexcomm 1: USART RTS, I2C SCL
			BLE_PTI0	O	BLE packet traffic information bit 0
			SPIFI_CLK	O	clock output for the SPI flash interface
PA05	33	PU	GPIOA5	I/O	general-purpose digital input output pin
			ADC3	AI	ADC external input 3
			SCT0_OUT5	O	SCTimer output 5
			CTIMER0_MAT1	O	32-bit CTimer 0 match output 1
			FC0_RXD	I/O	flexcomm 0: USART RXD
			FC2_SCL_MISO	I/O	flexcomm 2: SCL, SPI MISO
			SPIF_IO1	I/O	data bit 1 for the SPI flash interface
PA04	34	PU	GPIOA4	I/O	general-purpose digital input output pin
			ADC2	AI	ADC external input 2
			SCT0_OUT4	O	SCTimer output 4
			CTIMER0_MAT0	O	32-bit CTimer 0 match output 0
			FC0_TXD	I/O	flexcomm 0: USART TXD
			FC2_SDA_MOSI	I/O	flexcomm 2: I^2C SDA, SPI MOSI
			SPIF_IO0	I/O	data bit 0 for the SPI flash interface
PA03	35	PU	GPIOA3	I/O	general-purpose digital input output pin
			QDEC0_B	I	quadrature decoder 0 input channel B
			SCT0_OUT3	O	SCTimer output 3
			CTIMER0_MAT1	O	32-bit CTimer 0 match output 1
			R	O	reserved
			FC2_SDA_SSEL0	I/O	flexcomm 2: I^2C SDA, SPI SSEL0
			RFE_TX_EN	O	TX enable for external RF front-end
PA02	36	PU	GPIOA2	I/O	general-purpose digital input output pin
			QDEC0_A	I	quadrature decoder 0 input channel A
			SCT0_OUT2	O	SCTimer output 2
			CTIMER0_MAT0	O	32-bit CTimer 0 match output 0
			R	I/O	reserved
			FC2_SCL_SSEL1	I/O	flexcomm 2: I^2C SCL, SPI SSEL1
			RFE_RX_EN	O	RX enable for external RF front-end
NTAG_FD	37	—	—	O	field detection
VCC	38	—	—	—	power supply (1.62 V to 3.6 V)
NTAG_VCC	39	—	—	—	NTAG power supply
VOUT	40	—	—	—	output supply voltage(energy harvesting)

Table 2. Pin description *…continued*

Symbol	LFLGA54	Reset state[1]	Alternate function	Type	Description
VSS1	41	—	—	—	ground
PA01	42	PU	GPIOA1	I/O	general-purpose digital input output pin
			ADC1	AI	ADC external input 1
			SCT0_OUT1	O	SCTimer output 1
			CTIMER0_CAP1	I	32-bit CTimer 0 capture input 1
			FC0_CTS	I/O	flexcomm 0: USART CTS
			FC2_SSEL2	I/O	flexcomm 2: SPI SSEL2
			WLAN_RX	I	WLAN active high RX active indicator for coexistence
PA00	43	PU	GPIOA0	I/O	general-purpose digital input output pin
			ADC0	AI	ADC external input 0
			SCT0_OUT0	O	SCTimer output 0
			CTIMER0_CAP0	I	32-bit CTimer 0 capture input 0
			FC0_RTS	I/O	flexcomm 0: USART RTS
			FC2_SSEL3	I/O	flexcomm 2: SPI SSEL3
			WLAN_TX	I	WLAN active high TX active indicator for coexistence
PA31	44	PU	GPIOA31	I/O	general-purpose digital input output pin
			DAC	AO	DAC analog output
			RTC_CAP	I	RTC capture input
			CTIMER3_MAT2	O	Timer 3 match output 2
			SWO	I/O	serial wire trace output
			FC3_SCK	I/O	flexcomm 3: SPI clock
			SPIFI_CLK	O	clock output for the SPI flash interface
GND	45	—	—	—	ground
GND	46	—	—	—	ground
GND	47	—	—	—	ground
ANT_Pin3	48	—	—	—	Internal antenna ground
ANT_Pin2	49	—	—	—	Internal antenna ground
ANT_Pin1	50	—	—	—	Internal antenna ground
GND	51	—	—	—	ground
GND	52	—	—	—	ground
GND	53	—	—	—	ground
GND	54	—	—	—	ground

[1] PU = input mode, pull-up enabled (pull-up resistor pulls up pin to V_{CC}). Z = high impedance; pull-up or pull-down disabled, AI = analog input, AO = analog output, I = input, O = output, F = floating. Reset state reflects the pin state at reset without boot code operation. For pin states in the different power modes, see Section 7.2.2. For termination on unused pins, see Section 7.2.1.

5. QN9080-NTAG I²C Interface

5.1 Feature

- I²C master supported
- SCL clock speed configurable, up to 400 kb/s
- SCL direct push output
- 8-bit shift register for transform
- Internal bonding SDA pull-up, with pull-up resistor configurable

5.2 Basic Configuration

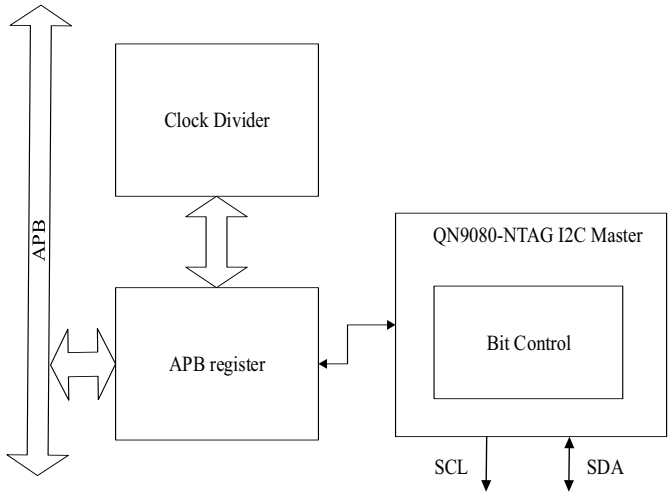

Fig 4. QN9080-NTAG I²C master

Configure the QN9080-NTAG I²C with the following steps:

1. Clear the QN9080-NTAG I²C peripheral reset by writing 1 to CLR_CHARG_RST register (bit 18 of RST_SW_CLR in SYSCON)
2. Set the CLK_CHARG_EN bit in the CLK_EN register of the SYSCON block to enable the clock of QN9080-NTAG I²C to start operating.
3. Typically, QN9080-NTAG I²C master is tied directly to the internal SIP-ed slave, where CHRG_SEL bit (bit 18) of PIN_CTRL_MISC should be set to 0. See Section 5.3 “Pin Description” for details.
4. Setup SCL clock speed by PRE_SCALE and CK_RATIO fields in CTRL register. See Section 5.5.1 “Clock” for details.
5. Set CHRG_EN bit in CTRL register to 1 to enable the peripheral to work.
6. If the master wants to send data to slave, the steps can be as follows:

a. Write slave address into TXD, including the read/write flag bit, which should be 0. Thus, the START in TXD is configured to tell the hardware to send an I2C START signal before sending the address byte. And the slave address is loaded into shift register.
b. The controller sets a start signal and slave address to I2C bus. After the setting data is sent and ACK from slave is received, the TX_INT happens.
c. Read the ACK_RECV in STAT, to see if there is an ACK. If there is an ACK, go to step d, otherwise go to step h.
d. Write new data to TXD register and set WR_EN in TXD register to 1, to declare next transfer is sending data out.
e. Clear interrupt. The data in TXD register is loaded into shift register.
f. Data in TXD register is clocked out to slave, after the ACK is received from slave, TX_INT happens, then goes to step c.
g. Set TOP in TXD register to 1, and clear TX_INT to 0, to generate a STOP waveform in I2C bus.
h. Wait until the bus is not busy.

7. If the master wants to receive data from slave, the steps can be as follows:
   a. Write slave address into TXD, including the read/write flag bit, which should be 1
   b. Set START in TXD. Thus, the slave address is loaded into shift register.
   c. The controller sets a start signal and slave address to I2C bus. After the setting data is sent, and ACK is received from slave, the TX_INT happens.
   d. Read the ACK_RECV in STAT, to see if there is an ACK.
   e. If this is not the last byte expected to receive, clear ACK_SEND to 0 in TXD, otherwise set ACK_SEND to 1. Clear interrupt, and set RD_EN in TXD to 1.
   f. Slave transfers data to master. Master clocks in data on I2C bus. After 8-bit data is received and ACK/NAK is send, RX_INT happens.
   g. Check RX_INT, and read data from RXD. If it is asserted, go on transfer to step e, otherwise go to step h.
   h. Set STOP in TXD and clear interrupt.
   i. Stop signal is transmitted on I2C bus.
   j. Wait until the bus is not busy.

5.3 Pin Description

QN9080-NTAG I2C master can be tied to either internal bonding slave or slave outside of chip, which is selected by PIN_MISC_CTRL[CHRG_SEL] bit:

Table 3. PIN_MISC_CTRL[CHRG_SEL] field descriptions

CHRG_SEL	Descriptions
0	QN9080-NTAG I2C master is tied to internal bonding slave
1	QN9080-NTAG I2C master is tied to pin mux.

When QN9080-NTAG I2C master is tied to pin mux, it can be tied to several pins, which is configured by PIO_FUNC_CTRL<x> register

Table 4. QN9080-NTAG I²C pin descriptions

Pin function	Type	Location	Description	Configuration
CHRG_SDA	I/O	PA02	Data line of I²C	PIO_FUNC_CTRL0<8:6> = 100
CHRG_SDA	I/O	PA13	Data line of I²C	PIO_FUNC_CTRL1<22:20> = 001
CHRG_SCL	O	PA03	Clock line of I²C	PIO_FUNC_CTRL0<11:9> = 100
CHRG_SCL	O	PA12	Clock line of I²C	PIO_FUNC_CTRL1<18:16> = 001

5.4 General Description

I²C bus controller supports some basic operations: start, stop, ack, and byte transfer. Master controller generates these basic operation commands, using an FSM. These commands are passed to bit control module which translates these commands into bus line operations.

So the QN9080-NTAG I²C controller has two FSMs: one is command level FSM, which is a main state machine, and the other is bit level FSM, which is a slave state machine.

Remark: QN9080-NTAG I²C is not a standard I²C master, where SCL line is direct output instead of pull-up and open-drained. So clock stretch and bus arbitration are not supported, where only point-to-point connection and transmission are considered in the application.

5.5 Function Description

5.5.1 Clock

There are two stages of I²C clock

- PRE_SCALE
- CK_RATIO

APB clock is firstly divided by PRE_SCALE register, and the division true table is shown as below:

Table 5. PRE_SCALE field descriptions

PRE_SCALE	Division
00	2
01	4
10	8
11	16

Divide the clock from the first stage, which is configured by CK_RATIO register.

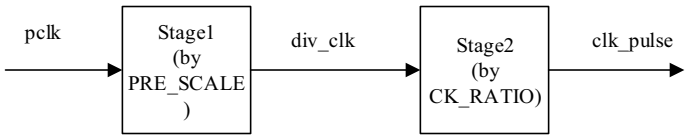

Fig 5. QN9080-NTAG clock generation

Then the I²C master SCL frequency can be calculated as:

$$f(SCL) = \frac{f(APB)}{\frac{2^{(PRESCALE+2)}/(CK\_RATIO+1)}{5}}$$

The duty factor of SCL is 2:3:

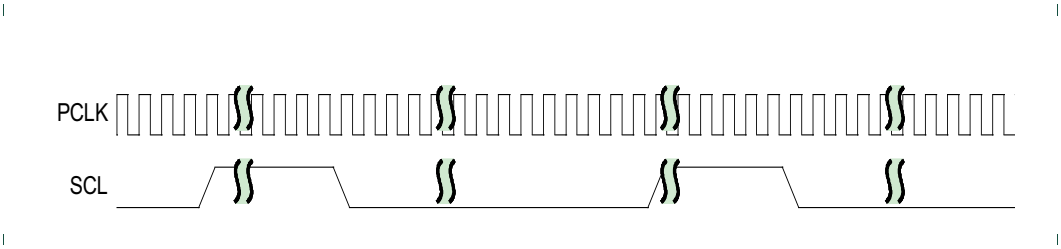

Fig 6. SCL clock generation

Then divider's counter can only be counted when the CHRG_EN is enabled.

5.5.2 Bit waveform

The controller generates basic bit-level waveform which is shown below. Each bit-operation is divided into 5 pieces: idle, A, B, C and D, except for the START operation which is divided into 6 pieces: idle, A, B, C, D and E. Each piece has the same time period.

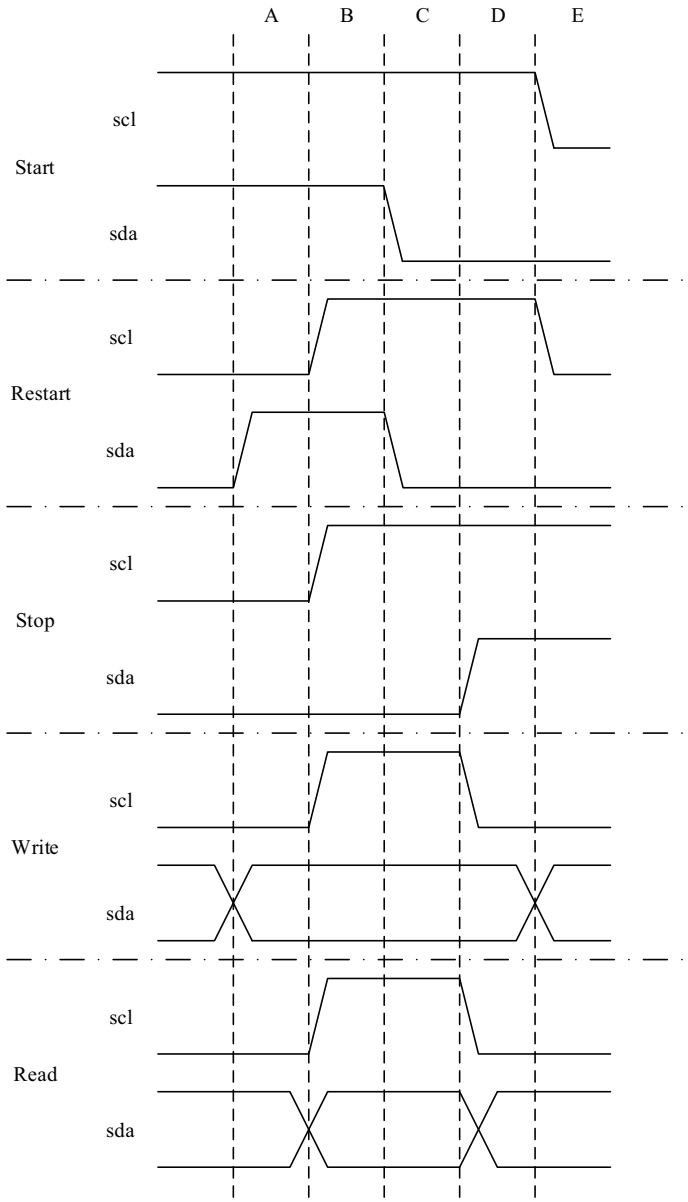

Fig 7. Bit waveform

While reading data from slave, master samples at the negative edge of SCL.

5.5.3 Internal Pull-up

When CHRG_SEL bit is 1, I^2C master is tied to pinmux, and the pull-up is controlled by PIO_PULL_CTRL<x> register.

When CHRG_SEL bit is 0, I^2C master is tied to internal bonding pins. At this time, SCL is directly output with one pull-up or pull-down resister, but SDA is pull-up, and the resister is configurable with CHRG_SDA_PULL bit in PIN_CTRL_MISC register:

Table 6. CHRG_SDA_PULL field descriptions

CHRG_SDA_PULL	Pull up resistor
00	5 kΩ
01	10 kΩ
10	20 kΩ
11	High-Z

5.6 Register description

Address offsets are within the address space of the related flexcomm interface. The reset value reflects the data stored in used bits only. It does not include reserved bits content.

Table 7. I^2C-bus register overview

Name	Access	Offset	Description	Reset value	Section
CTRL	RW	0x000	Control register	0x0	5.6.1
STATUS	RW	0x004	Status register	0x0801	5.6.2
TXD	RW	0x008	Transmitting data register	0x0	5.6.3
RXD	WO	0x00C	Receiving data register	NA	5.6.4
INT	RW	0x010	Interrupt register	0xFFFF	5.6.5

5.6.1 Control register

Table 8. CTRL - control register (offset = 0x000) bit description

Bit	Symbol	Value	Description	Reset Value	
0	TX_INT_EN		TX interrupt enable	0x0	RW
		0	disabled; The TX interrupt is disabled		
		1	enabled; the TX interrupt is enabled		
1	RX_INT_EN		RX interrupt enable	0x0	RW
		0	disabled; the RX interrupt is disabled		
		1	enabled; the RX interrupt is enabled		
2	CHRG_INT_EN		QN9080-NTAG I^2C interrupt enable	0x0	RW
		0	disabled; the QN9080-NTAG I^2C interrupt is disabled		
		1	enabled; the QN9080-NTAG I^2C interrupt is enabled		
7:3	RESERVED	-	read value is undefined, only zero should be written	-	RO
8	CHRG_EN		QN9080-NTAG I^2C enable	0x0	RW
		0	disabled; QN9080-NTAG I^2C is disabled		
		1	enabled; QN9080-NTAG I^2C is enabled.		
23:9	RESERVED	-	read value is undefined, only zero should be written	-	RO
29:24	CK_RATIO		I^2C master clock ratio (second stage of clock divider, see Section 5.5.1 "Clock" for detail)	0x0	RW

Table 8. CTRL - control register (offset = 0x000) bit description

Bit	Symbol	Value	Description	Reset Value	
31:30	PRE_SCALE		I2C master clock pre scale (see Section 5.5.1 “Clock” for detail)	0x0	RW
		0x0	divide by 2		
		0x1	divide by 4		
		0x2	divide by 8		
		0x3	divide by 16		

5.6.2 Status register

Table 9. STATUS - status register (offset = 0x004) bit description

Bit	Symbol	Value	Description	Reset value	Access
0	ACK_RECV		Ack received	0x1	RO
		0	Ack is not received		
		1	Ack is received		
1	BUSY		I2C busy	0x0	RO
		0	I2C is not busy		
		1	I2C is busy		
31:2	RESERVED	-	read value is undefined, only zero should be written	-	-

5.6.3 Transmitting data register

Table 10. TXD - Transmitting data register (offset = 0x008) bit description

Bit	Symbol	Value	Description	Reset value	Access
7:0	I2C_TXD		I2C send data	0x0	RW
15:8	RESERVED	-	read value is undefined, only zero should be written	-	
16	START		I2C start, this bit only generate a pulse to start the state machine.	0x0	W1
17	STOP	-	I2C stop, this bit automatically pulls down while stop signal is finished.	0x0	W1
18	WR_EN		Write transfer enable, this bit only generate a pulse to start the state machine	0x0	W1
		0	disabled; the write transfer is disabled		
		1	enabled; the write transfer is enabled		
19	RD_EN		Read transfer enable, this bit only generate a pulse to start the state machine	0x0	W1
		0	disabled; the read transfer is disabled		
		1	enabled; the read transfer is enabled		
20	ACK_SEND		ACK send	0x0	RW
		0	ACK is not sent		
		1	ACK is sent		
31:21	RESERVED	-	read value is undefined, only zero should be written	-	

5.6.4 receiving data register

Table 11. RXD - receiving data register (offset = 0x00C) bit description

Bit	Symbol	Description	Reset value	Access
7:0	I2C_RXD	I^2C receive data	0x0	RO
3:1	RESERVED	read value is undefined, only zero should be written	-	

5.6.5 Interrupt register

Table 12. INT - Interrupt register (offset = 0x010) bit description

Bit	Symbol	Description	Reset value	Access
0	TX_INT	TX interrupt	0x0	W1C
1	RX_INT	RX interrupt	0x0	W1C
2	CHRG_INT	QN9080-NTAG I^2C interrupt	0x0	RO
31:3	RESERVED	read value is undefined, only zero should be written	-	

6. QN9080 User Manual

QN908x user manual introduces the details of QN9080. You can always get the latest QN908x User Manual at NXP website. Go to nxp.com and perform a search of UM11023, you will get QN908x user manual.

7. NTAG Data Sheet

NT3H2111_2211 Product Data Sheet introduces the information about the NTAG, you can always get the latest NT3H2111_2211 at NXP website. Go to nxp.com and perform a search of 359932, you will get NT3H2111_2211 Product Data Sheet.

8. Abbreviations

Table 13. Abbreviations

Acronym	Description
ADC	Analog-to-Digital Converter
AGC	Automatic Gain Control
AHB	Advanced High-performance Bus
AMBA	Advanced Microcontroller Bus Architecture
APB	Advanced Peripheral Bus
API	Application Programming Interface
BOD	Brown-Out Detector
BOR	Brown-Out Reset
BSDL	Boundary-Scan Description Language

Table 13. Abbreviations *…continued*

Acronym	Description
CRC	Cyclic Redundancy Check
CS	Capacitive Sense
DCC	Debug Communication Channel
DMA	Direct Memory Access
ETM	Embedded Trace Macrocell
FIFO	First-In, First-Out
FMC	Flash Memory Controller
FRO	Free-Running Oscillator
FSP	Fusion Signal Processing
GPIO	General Purpose Input/Output
I2C or IIC	Inter-Integrated Circuit bus
IAP	In-Application Programming
I2S	Inter-IC Sound or Integrated Interchip Sound
ISP	In-System Programming
ISR	Interrupt Service Routine
JTAG	Joint Test Action Group
LIN	Local Interconnect Network
NVIC	Nested Vectored Interrupt Controller
PDM	Pulse Density Modulation
PLL	Phase-Locked Loop
PMU	Power Management Unit
POR	Power-On Reset
PWM	Pulse Width Modulator
RAM	Random Access Memory
RCO	RC Oscillator
SPI	Serial Peripheral Interface
SRAM	Static Random Access Memory
SWD	Serial-Wire Debug
TAP	Test Access Port
USART	Universal Synchronous/Asynchronous Receiver/Transmitter
WOO	Write Only One
W1C	Write 1 to Clear

9. References

[1] **Cortex-M4 TRM —** Arm Cortex-M4 Processor Technical Reference Manual

[2] **Cortex-M0+ TRM —** Arm Cortex-M0+ Processor Technical Reference Manual

[3] **AN11538 —** AN11538 application note and code bundle (SCT cookbook)

[4] **UM10204 —** I^2C-bus specification and user manual

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11. Tables

12. Figures

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