

# UM1760 User manual

## STLUX<sup>™</sup> SMED configurator 1.0

#### Introduction

The STLUX SMED configurator is a powerful graphical tool which allows to easily configure the SMED engine embedded in the STLUX family of devices. The tool allows the user to focus on creating new SMED algorithms while completely reduces the implementation time end efforts. Once the visual SMED configuration is in place, the SMED configurator can generate a C file and store the whole configuration, ready to be imported in STLUX projects.

The SMED configurator features:

- SMED configuration schemes
- Input configuration
- Clock settings
- FSM ("Finite State Machine") configuration
- C code generation

## Contents

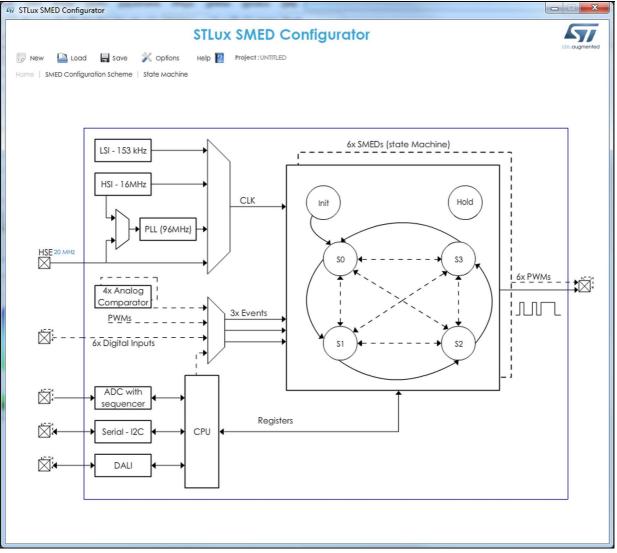
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## 1 Home page

The initial view gives a visual overview of the STLUX architecture. The user can interact with all the elements of the home page and access more detailed views for each component.







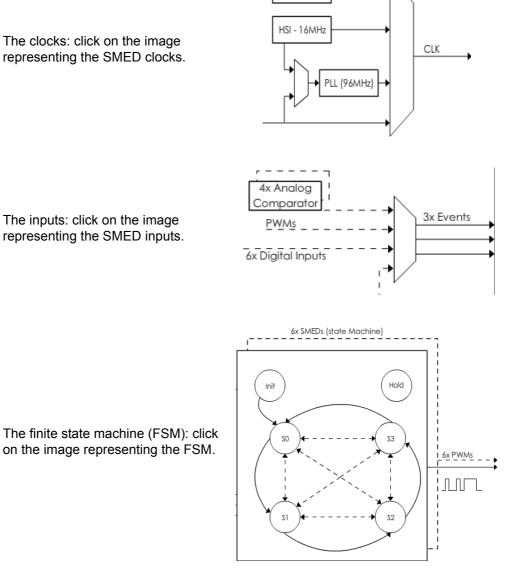
The user can choose to configure:

The clocks: click on the image • representing the SMED clocks.

The inputs: click on the image representing the SMED inputs.

on the image representing the FSM.

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LSI - 153 kHz

Alternatively, it is possible to use the top menu to jump into the desired view of the SMED configurator.

#### Figure 2. Menu bar

Home	SMED configurator Scheme	State Machine
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### 2 SMED configuration scheme view

This view allows the user to establish how to use each SMED defining its working mode.

All the possible SMED configuration schemes are:

- Single SMED
- Synchronous coupled SMEDs
- Two synchronous coupled SMEDs
- Two asynchronous coupled SMEDs
- Asynchronous coupled SMEDs
- Externally controlled SMED

The page shows the six SMEDs and for each of them there is a button to enable it and a button to choose the control mode (internally/externally). Each SMED, if not coupled to another, will be configured respectively in the SINGLE mode or EXTERNAL depending on whether the control button is either "Int" (internal) or "Ext" (external).



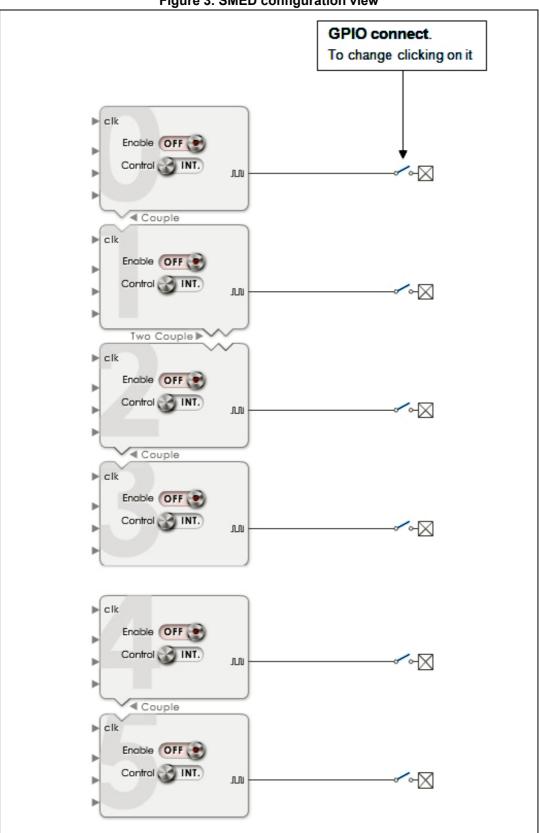
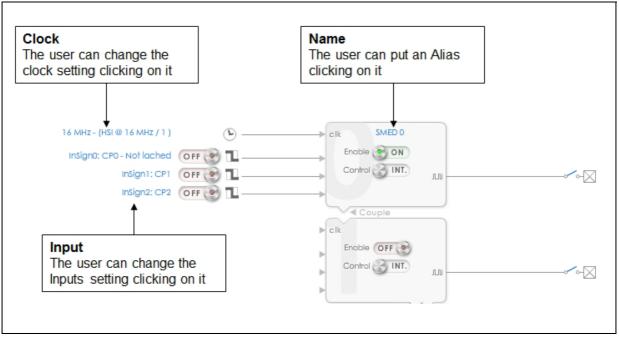


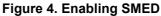
Figure 3. SMED configuration view

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Enabling a SMED will be shown:

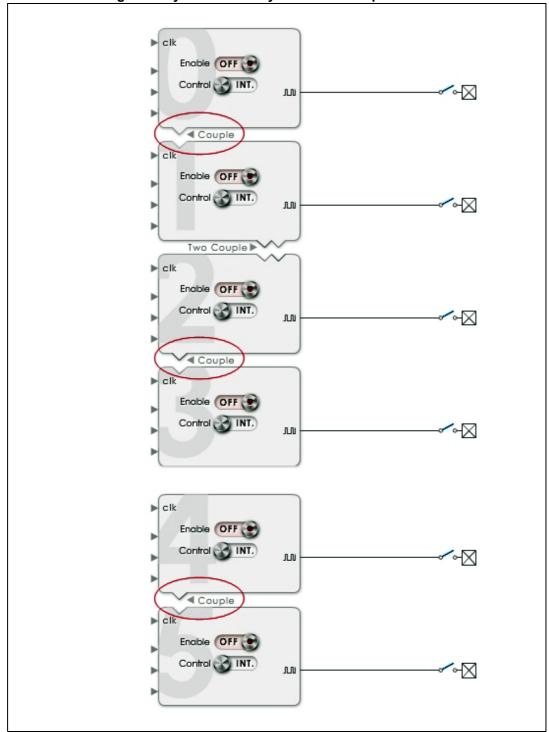


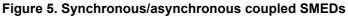




#### 2.1 Synchronous/asynchronous coupled SMEDs

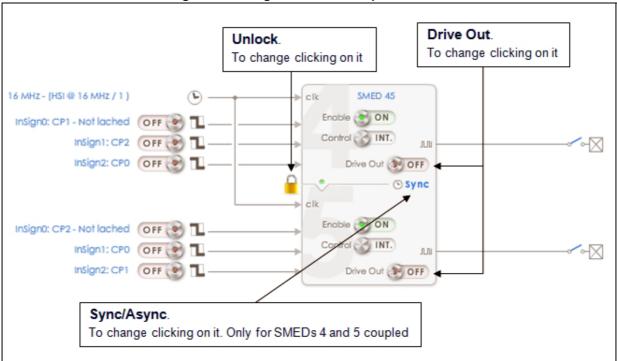
To configure 2 SMEDs in coupled mode, click the "couple" text between the 2 SMEDs required to be coupled.

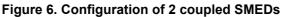






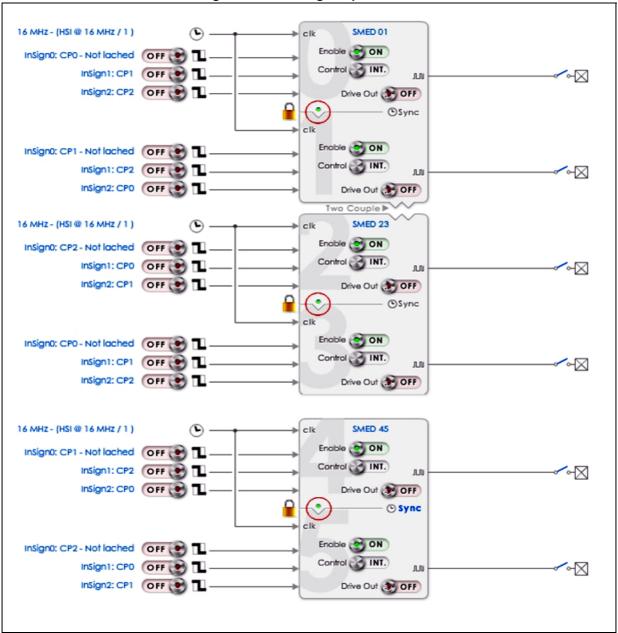
The result is that the tool shows graphically the 2 SMEDs coupled and allows the user to configure their features:







To remove the coupled mode click click on the symbol that shows the coupling of the SMEDs.







### 2.2 Two synchronous/asynchronous coupled SMEDs

To configure 4 SMEDs (SMED0 - SMED 1 - SMED 2 - SMED 3) into the two coupled mode it's needed to click on the area representing this mode:

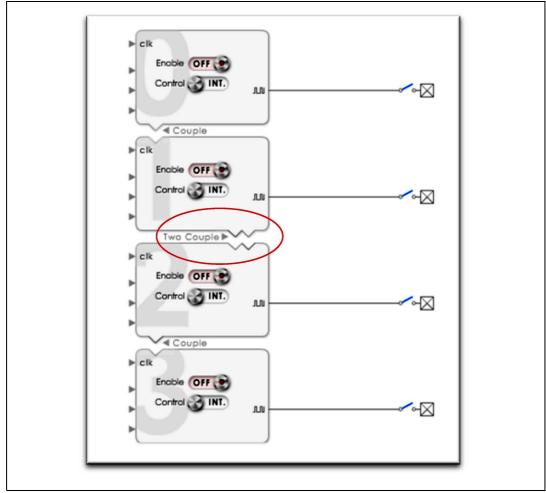


Figure 8. Configuring 4 SMEDs into two coupled mode



As a result, the SMED configurator shows graphically the 2 SMEDs coupled and allows the user to configure their features.

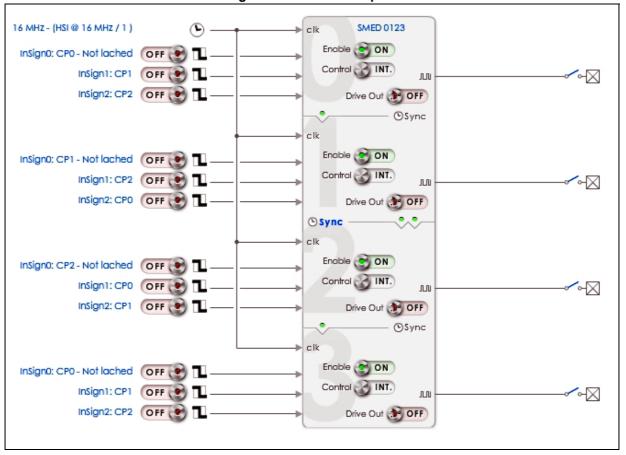
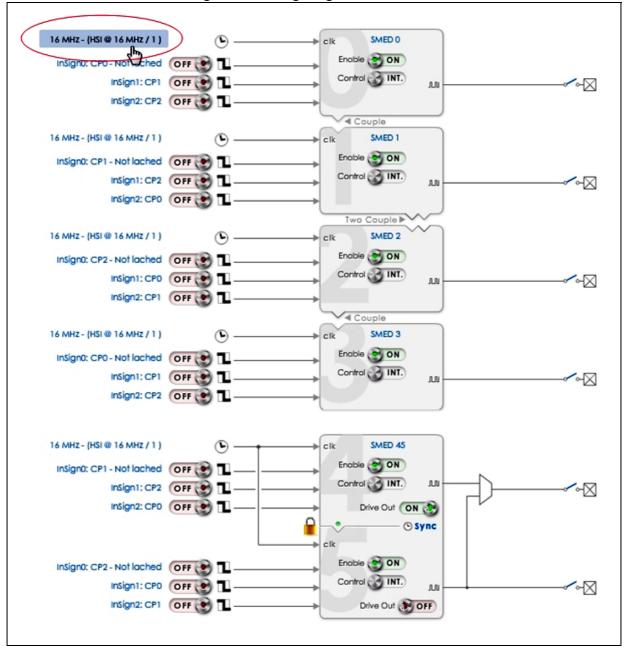


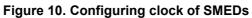
Figure 9. 2 SMEDs coupled



#### 2.3 Clock setting

Once a SMED configuration scheme has been selected, it is possible to configure the clock of the used SMEDs clicking on the clock label.







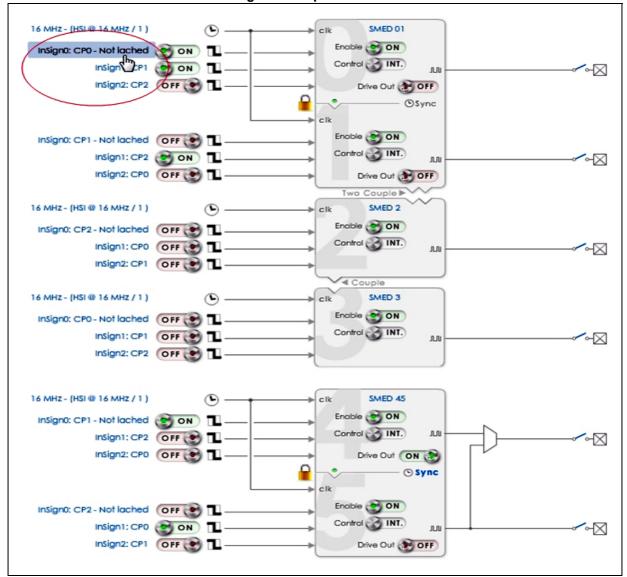
A dialog will be open in order to select one of the all possible values for the clock:

Clash for CHIED OI			Distance of		
Clock for SMED 01			HSEC	Clock setting <	<
High Speed Extern	nal Clock settings				
Contiguration ()	PLL input reference	auxiliary clock line			
Frequency	20				
PARE INCOMPTION					
material	on 1	Internal/External	Contra Samo	Divisor	
		Internal/External internal		Divisor	
Frequency 1 V	Clock source		Period	Divisor 1 2	F
Requency 1 V 96 MHz	Clock source PLL @ 96 MHz	internal	Period 10.42 ns	1	
Requency 1 V 96 MHz 48 MHz	Clock source PLL @ 96 MHz PLL @ 96 MHz	internal internal	Period 10.42 ns 20.83 ns	1	
Requency 1 V 96 MHZ 48 MHZ 24 MHZ	Clock source PLL @ 96 MHz PLL @ 96 MHz PLL @ 96 MHz	internal internal internal	Period 10.42 ns 20.83 ns 41.67 ns	1 2 4	
Prequency 1 V 96 MHz 48 MHz 24 MHz 20 MHz	Clock source PLL @ 96 MHZ PLL @ 96 MHZ PLL @ 96 MHZ HSE @ 20 MHZ	internal Internal Internal external	Period 10.42 ns 20.83 ns 41.67 ns 50 ns	1 2 4 1	
Requency         1 ▼           96 MHZ         48 MHZ           48 MHZ         24 MHZ           24 MHZ         20 MHZ           16 MHZ         16 MHZ	Clock source PLL @ 96 MHZ PLL @ 96 MHZ PLL @ 96 MHZ HSE @ 20 MHZ HSE @ 16 MHZ	internal internal external internal	Period 10.42 ns 20.83 ns 41.67 ns 50 ns 62.5 ns	1 2 4 1	



#### 2.4 Input setting

Once a SMED configuration scheme has been selected, it is possible to configure the inputs of the used SMEDs by clicking the "input" label.







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A dialog will be open in order to configure the three inputs of the selected SMED.

Liqura	12	Innut	adjantion	dialaa
rigure	13.	mpuι	selection	ulalog

nputs s		i lane	1		- 10-23	1017.	oone 🖹
MED 0							
	Enable	Control	Level	Alias			
Insign0	ON	CPO	Low Level	STOP		Not lached	
Insign 1	ON	DIG3	Rising Edge	Sense CUr	•		
InSign2	OFF .	CP2	T Falling Edge	InSign2			

It is possible to enable an input by clicking the ON/OFF button:

Also it is possible to change the input trigger level by clicking on the trigger icon:

A menu with the 4 possible values will be opened:

1		1
ł	T Falling Edge	
t	Rising Edge	1
	Low Level	
÷	High Level	T
١.		- 4



It is also possible to enable the InSig[0] input line supplementary latch functionality used to memorize occurrence of an InSig[0] capture condition.

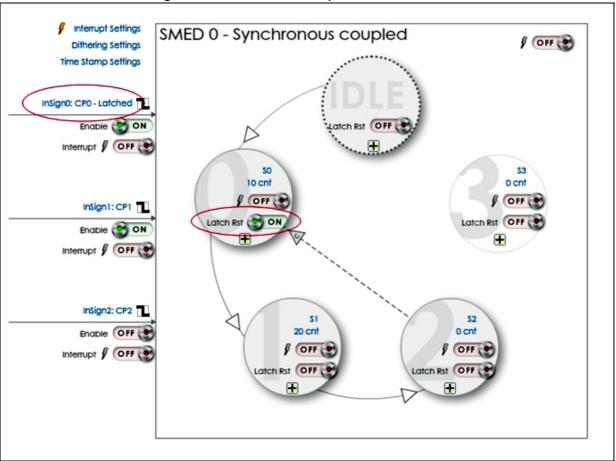
				10		
MED 0						
	Enable	Control	Level	Alias		
InSign0	ON	CPO	Low Level	STOP	Lotche	d de
In\$ign1	ON	DIG3	Rising Edge	Sense CUr	•	
Insign2	OFF 💽	CP2	T Falling Edge	Insign2		

Figure 14. Enabling Sig[0] latched mode

This allows a deferred event transition occurrence from any of the configured states to react to the InSig[0] input capture.



The latched information is selectively cleared by entering any of the S0 - S3 states if the latch reset for the state is set in the correspondent SMED state machine page.







## 3 State machine page

The machine states page is used to set the configuration of the SMED registers that control the finite state machine.

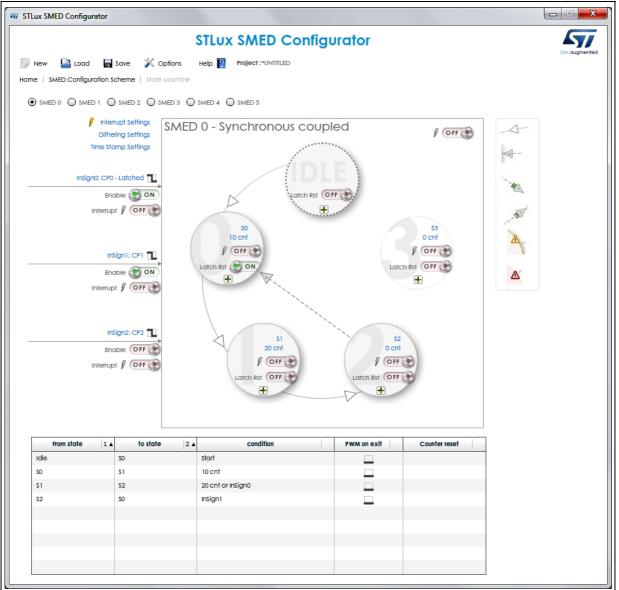


Figure 16. Finite state machine (FSM) view

This page is divided into 2 parts:

- General settings
  - a) Interrupt
  - a) Dithering
  - a) Time stamp
- 2. Transitions

1.



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#### 3.1 General setting

#### 3.1.1 Interrupt settings

The "interrupt settings" label is used to configure the interrupt handling.

Clicking on the label "Interrupt Settings" a dedicated window will be opened.

The interrupts are grouped in three blocks for the state timers compare events, external input events and counter overflow event.

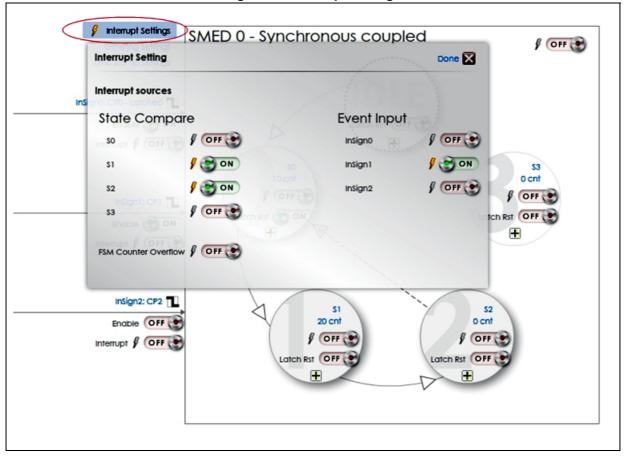


Figure 17. Interrupt settings



#### 3.1.2 Dithering settings

The "dithering settings" label is used to determine the SMED cycle(s) in which the temporary dithering increment is applied on the selected timer. Any number of cycles may be enabled/disabled.

Clicking on the label "Dithering Settings" a dedicated window will be opened.

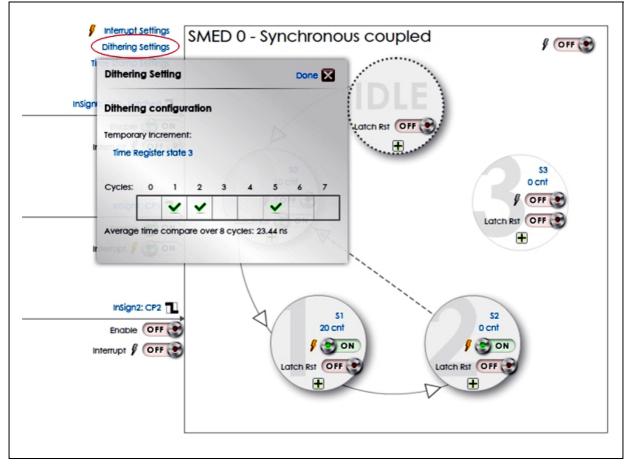


Figure 18. Dithering settings



#### 3.1.3 Time stamp settings

The "time stamp settings" label is used to control the dumping feature of the SMEDs. Clicking on the label "time stamp settings" a dedicated window will be opened.

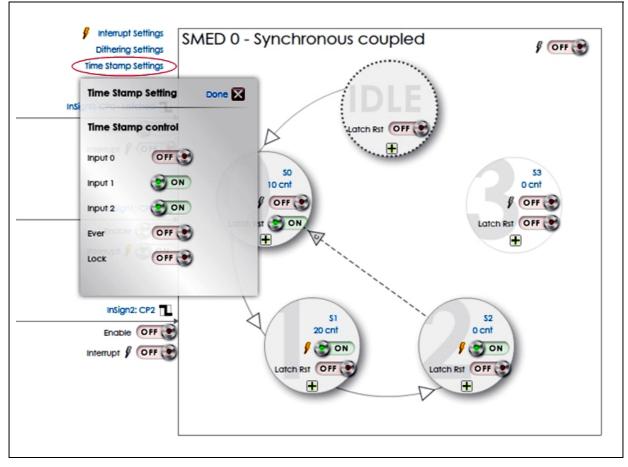


Figure 19. Time stamp settings



#### 3.2 Transitions

State transitions are represented as arrows connecting two states involved in a transition.

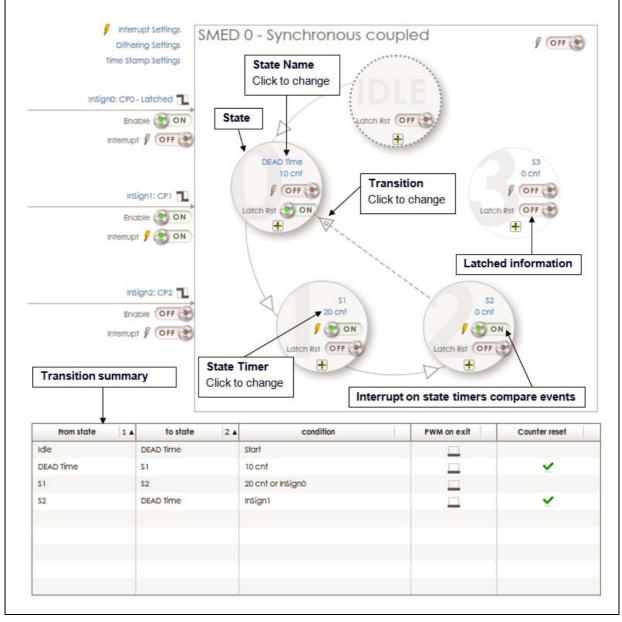


Figure 20. State transitions



To add a new transaction, click on the button  $\blacksquare$  relative to the initial state of the transition. A dedicated window will be opened to select the end state of the transition.

Transition settings - SMED 0 - Synchronous coupled	
Transition settings - SMED 0 - Synchronous coupled	
Path	
From State: S0 🔻	To State:
0	
Condition	
Action	
	OK Cancel

Figure 21. Selecting end state of the transition

To define a transition **three steps** are needed:

1. Path:

Determine the path of the transition from the initial state to the end state. The tool automatically determines the type of transition (sequential or controlled) or, in case of ambiguity, leaves the choice to the user.

- 2. Condition Determine which is the condition that generates the transition: the state compare timer, edgeX triggering event, edgeY triggering event and their combination.
- 3. Action Determine which is the action of the transition in term of the PWM value and reset counter.



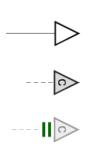
Transition settings - SMED 0 - Synchronous co	pupled	
fransition settings - SMED 0 - Synchro	nous coupled	
Path		
From State: S0 🛛 🔻		To State: S2 🔻
UL DIOH	sequential > OFF controlled > (2) ON and Hold Exit Imp waking up when the same condition of the this transition will be retriggered	
UL DIOH	add that has the corresponding add the corre	
CMPL	EDGE	EDGE
Use it OFF	Use it OFF	Use it ON
10 🐼 cnt 🤎	Insign0 (O) Insign1 Insign2	Insign 1 Insign 2
Action PWM:		
		OK Cancel

Figure 22. Transition definition

For the controlled transition the user can enable the possibility to enter the hold state and decides which is the condition that determines the exit from the hold state to go on the end state of the transition.



The tool uses four different symbols to identify the transition:



Sequential transition

Controlled transition

Controlled transition with the hold jump and exit from the hold when the same condition is retriggered.

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Controlled transition with the hold jump and exit from the hold when a coupled SMED enters in hold.



### 4 Menu bar

The menu bar contains the commands that can be used to manage the application.

The available menus are:

- New
  - Create a new project
- Load

Load existing project

- Save
  - Save

Save the active project

Save As…

Save the active project with a new name

Save C File

Save the text file, that contains the "C" source code of a simple function that initializes all the MIF and SMED registers conforming to the current configuration.

• Option

Open the Option window

- Help
  - Help

Open this file

- Release Note
  - Open the Release Note document
- About

Open the About window.



## 5 Revision history

Table 1.	Document	revision	history
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Date	Revision	Changes
14-May-2014	1	Initial release.



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