UM2297
User manual

Getting started with the STEVAL-IFP029V1 for the IPS4260L high speed quad low-side driver with dedicated GUI

Introduction

The STEVAL-IFP029V1 is an evaluation board designed to analyze the functions of the IPS4260L fast quad low-side intelligent power switch. The application board has been designed to meet the industrial standard requirements concerning:

1. Galvanic isolation between logic and power stages.
   High speed dual channel optocouplers have been used both for signals forwarded to the device and for feedback signals.
2. Reverse polarity protection.
   V_{CC} (power stage) supply voltage is protected versus reverse polarity by D1.
   Reverse polarity protection is implemented for the logic stage supply voltage (V_{DD}) by D8.
3. EMC requirements (surge, burst and ESD).
   On board TVS devices on V_{CC}, V_Z and V_{DD} (U8, U2 and U9, respectively) clamp overvoltage for surge test. The STEVAL-IFP029V1 meets IEC61000-4-2, IEC61000-4-4 and IEC61000-4-5 industrial standards.

Contents

1 Overview

This dual layer design meets the thermal requirements of the application: dedicated copper areas reduce Z_{th} and then enhance the thermal dissipation response when the device is used in switching mode. The integrated channel-independent thermal protection of the IPS4260L is reported to the user by turning on the red LED D3. The R17, R18, R19 and R20 resistors activate the open load detection feature integrated in the IPS4260L: the red LED D2 is turned on if one, or more, of the four outputs are left open. The board mounts four green LEDs (D4, D5, D6 and D7), one for each of the four output stages: each green LED turns on once the correspondent channel is activated. Some features can be modified by few changes in the application components. For example the default current limitation threshold can be modified through R23, while the cut-off duration time (default = 2 ms) can be modified through R4 (refer to the IPS4260L datasheet for the selection of R4 and R23). The IPS4260L can be driven by a user friendly (STSW-IFP029GUI available on www.st.com) by connecting the STEVAL-IFP029V1 through the STEVAL-PCC009V2 to a Win OS laptop/PC.

Figure 1: STEVAL-IFP029V1 evaluation board

2 Board features

- Dedicated voltage supply for logic (V_{DD}) and power (V_{CC}) stages
- V_{CC} operating voltage from 8 V to 36 V
- V_{DD} operating voltage range 3.3 V to 5 V
- Default limitation current 1 A per channel
- Default cut-off delay time 2 ms
- Max. switching frequency
- High speed opto-isolation for driving and feedback diagnostics
- Red LED for thermal and cut-off channel status signalization
- Red LED for open load detection in OFF-state
- Thermal shutdown
- Reverse polarity protection
- Designed to meet EMC standard requirements: IEC61000-4-2, IEC61000-4-4, IEC61000-4-5

3 Board description

The table below summarizes the connectors and test points available on the board.

Table 1: STEVAL-IFP029V1 connector and jumper description

Name	Type	Function	Details
J6	3-way screw connector	V_{CC} and V_{DD} and supply voltages	PIN1: V_{DD} PIN2: GND PIN3: V_{CC}
J7	4-way screw connector	Output connector	PIN1: OUT1 PIN2: OUT2 PIN3: OUT3 PIN4: OUT4
CN1	30-pin flat connector	Connection for STEVAL-PCC009V2	See table below
J1, J2, J3, J4	Drop jumpers	When closed, they enable the transmission of the INx status to CN1 (fault CH1, fault CH2, fault CH3, fault CH4)	Default: J1 closed J2 closed J3 closed J4 closed
J5, J8, J9	Drop jumpers	The default condition enables U2 between V_Z and V_{CC}. U2 is the TVS protecting the OUTPUT pins despite surge up to ±2 kV. Also, it allows the maximum inductive load capability to be increased	Default: J5 open J8 open J9 closed
J10	Drop jumper	If closed it enables U8, the TVS protecting V_{CC} despite the surge up to ±2 kV	Default closed
J11	Drop jumper	Disconnect V_{DD} path	Default closed
TP1	Test point	Logic stage GND	MCU_GND
TP2	Test point	IPS4260L, $\overline{OL}$ pin	Active low
TP3	Test point	IPS4260L, $\overline{FLT}$ pin	Active low
TP4, TP5, TP6, TP7	Test point	IPS4260L IN1, IN2, IN3, IN4 pins	

Table 2: STEVAL-IFP029V1 30-pin signal connector description

Pin number	Description
1	NC
2	MCU_GND
3, 4, 5, 6	NC
8	Digital input IN1/PWM1
7	Digital input IN2/ PWM1
9, 10, 11, 12	NC
13	MCU_GND
14	MCU_VDD
15	Fault CH1
16	Fault CH2
17	Fault CH3
18	Fault CH4
19	Digital input IN3/ PWM2
20	FAULT_FLT (global cut-off/thermal fault)
21	Digital input IN4/ PWM2
22	FAULT_OL (global open load fault)
23	NC
24, 25	Digital acknowledge
26, 27	NC
28	MCU_GND
29, 30	NC

Figure 2: STEVAL-IFP029V1 schematic

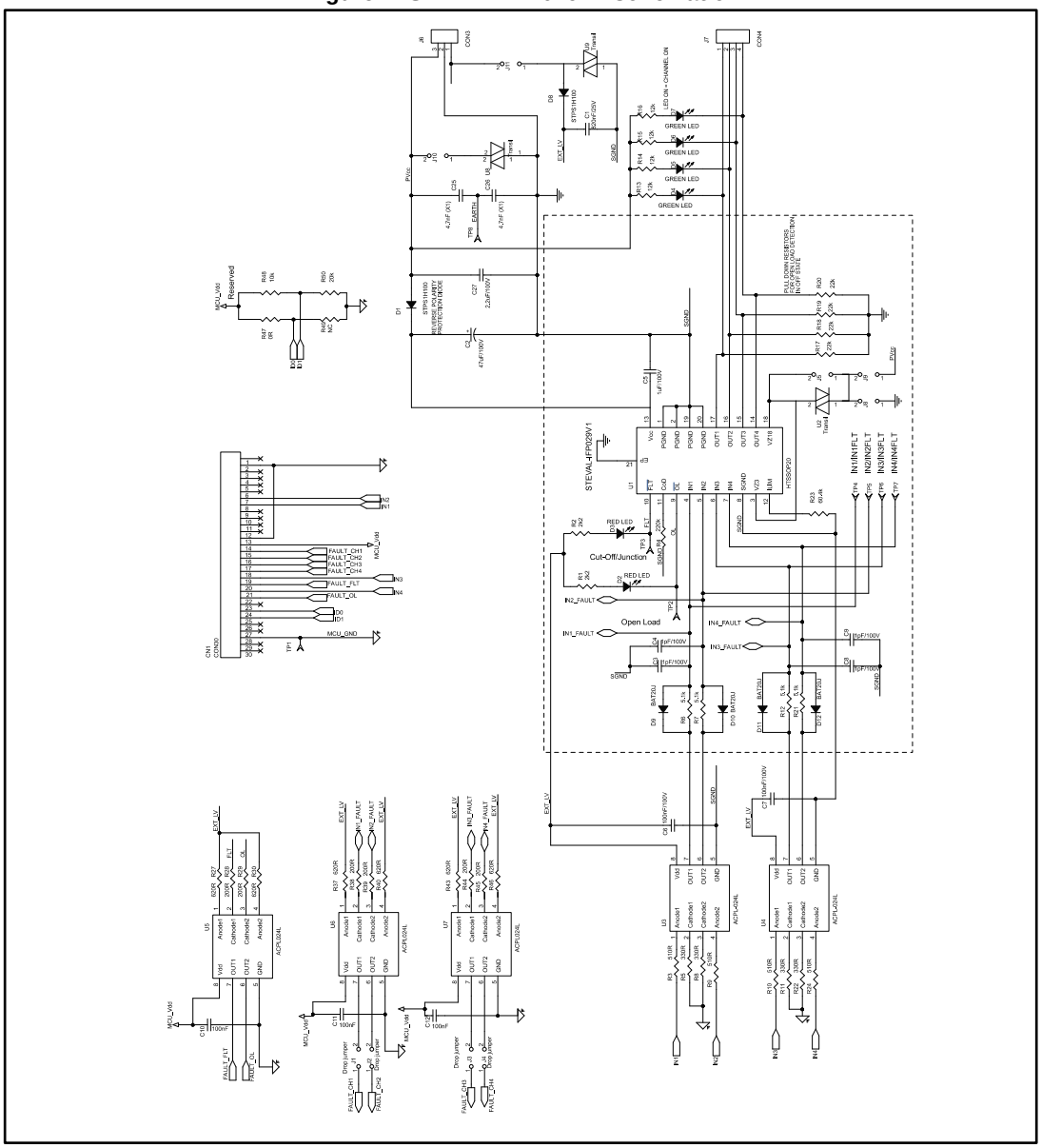


Table 3: STEVAL-IFP029V1 bill of material

Item	Q.ty	Ref.	Part/Value	Description	Manuf.	Order code
1	1	CN1	CON30	2.54 mm 30 pins (15x2 rows)	FCI	52601-S30-4LF
2	1	C1	820 nF 25 V ±10%	X7R	AVX	12063C824KAT2A
3	1	C2	47 uF 100 V ±20%	Electrolityc	Rubycon	100ZL47MEFC10X12.5
4	4	C3,C4,C8, C9	1 pF 100 V ±25%	COG	MURATA	GQM1885C2A1R0CB01D
8	1	C5	1 uF 100 V ±10%	X7R	AVX	12061C105KAT2A
9	5	C6,C7,C10, C11,C12	100 nF 100 V ±10%	X7R	MURATA	GRM188R72A104KA35D
14	2	C25, C26	4.7 nF 4 kV	Ceramic X1 class suppressor	VISHAY	VY1472M63Y5UG63V0
16	2	D1,D8	STPS1H100U		ST	STPS1H100U
18	2	D2,D3	Red LED 2.4 V	AlInGaP	WURTH	150060SS75000
20	4	D4,D5,D6, D7	Green LED 2.4 V	AlInGaP	WURTH	150060VS75000
24	4	D9,D10,D11, D12	BAT20J VRRM =20 V VF = 0.25 V		ST	BAT20JFILM
28	4	J1,J2,J3,J4,	Drop jumper			
32	5	J5, J8, J9, J10,J11				
36	2	R1,R2	2k2 0.1 W 0.1%		PANASONIC	ERA3AEB222V
41	4	R3,R9,R10, R24	510R 0.1 W 0.1%		PANASONIC	ERA3APB511P
43	4	R5,R8,R11, R22	330R 0.1 W 0.1%		PANASONIC	ERA3AEB331V
47	1	R4	220 k 0.1 W 0.1%		PANASONIC	ERA3AEB224V
51	1	R23	60.4 k 0.125 W 0.1%		TE CONN	RP73PF1J60K4BTDF
52	4	R17,R18, R19,R20	22 k 0.125 W 0.1%		Arcol	ACPP080522KBE
53	4	R6,R7,R12, R21	5 k1 0.25 W 1%		PANASONIC	ERJPA3F5101V
57	4	R13,R14, R15,R16	12 k 0.25 W 0.1%		PANASONIC	ERA8AEB123P
61	6	R27,R30, R37,R40, R43,R46	620R 0.25 W 1%		PANASONIC	ERJPA3F6200V

Item	Q.ty	Ref.	Part/Value	Description	Manuf.	Order code
65	6	R28,R29, R38,R39,R44,R45	200R 0.25 W 1%		PANASONIC	ERJPA3F2000V
71	1	R47	0 0.1 W 5%		YAGEO	232270296001
77	1	R48	10 k 0.1 W 0.1%		BOURNS	CRT0603-BY-1002ELF
78	0	R49 (DNM)				
79	1	R50	20 k 0.1 W 0.1%		VISHAY	MCT06030D2002BP100
79	8	TP1,TP2,TP3,TP4,TP5, TP6,TP7, TP8	Ring test point		KEYSTONE	5001
80	5	U3, U4, U5, U6, U7	OPTO_5 MHz ACPL-024L		Avago Technologies	ACPL-024L-000E
88	2	J7	4-way screw connector		TE CONN	282836-4
93	1	J6	3-way screw connector		RS	790-1174
95	1	U1	IPS4260L		ST	IPS4260L
96	1	U8	SMC30J33CA 3 kW		ST	SMC30J33CA
97	1	U2	SMC30J18CA 3 kW		ST	SMC30J18CA
98	1	C27	2 u 2 F 100 V	X7R	MURATA	GRM32ER72A225KA35L
99	1	U9	SM6T6V8CA 600 V		ST	SM6T6V8CA

3.1 Supply voltage section

The STEVAL-IFP029V1 needs two different supply voltages for logic stage (V_{DD}) and power stage (V_{CC}).

The V_{DD} voltage supplies the optocouplers and pulls up the red LEDs D2 and D3: the maximum admissible voltage is 5.5 V. The V_{CC} voltage can range between 8 V to 36 V. The operating range can be extended to 50 V but the TVS U8 must be disconnected by opening J10 or replaced by a proper one. Removing the TVS on V_{CC}, the ±2 kV surge protection is not guaranteed.

3.2 Communication

The galvanic isolation between the logic stage and the power stage is guaranteed by the high speed dual channel optocouplers (U3, U4, U5, U6 and U7).

Driving signals (from the micro controller to the IPS4260L) are handled by U3 and U4. Feedback signals (from the IPS4260L to the microcontroller) are handled by U5, U6 and U7. When the GUI and the STEVAL-PCC009V2 are used, two different modes can be selected based on the test the user wants to verify:

1. Simple ON/OFF mode
2. PWM mode

In PWM mode, the user can set channel frequency and duty cycle and activate/deactivate PWM mode for each channel.

3.3 Reverse polarity

The reverse polarity event happens when the user supplies the application board having wrongly swapped the polarity of the supply cables.

The application board is protected despite this undesired and destructive event by D1, placed in series to V_{CC} rail. D1 avoids that a huge current starts flowing through the IPS4260L, damaging the device itself.

Reverse polarity protection on V_{DD} is implemented as well as through the diode D8.

3.4 Open load detection

The IPS4260L embeds the open load in OFF-state detection feature. Due to this feature, during OFF-state (input low), it is possible to detect whether the load is disconnected or not, this detection is transferred to the user by the OL fault pin. (D2 turns on the STEVAL-IFP029V1).

To use this feature, a pull-down network (R17, R18, R19 and R20) is connected on output pins such that output pin voltage goes lower than V_{CC}-3.5 V (typ.) when the load is disconnected.

4 Power dissipation

The IC is self-protected against overheating by thermal junction protection. The exposed pad of the IC is soldered to the copper areas on top and bottom sides (connected through vias) allowing a proper heatsink capability.

Special care must be taken to thermal effects when the board is used in PWM mode at high switching frequency. The power dissipation increases proportionally to the load current, switching frequency, and number of channels used.

At high frequency, a considerable power dissipation capability is necessary because otherwise the junction temperature could increase up to a regime value that exceeds the device thermal shutdown.

When it happens the device stops the switching until the temperature decreases under the restart value.

The following table summarizes the power dissipation performance of the STEVAL-IFP029V1 at T_{amb} = 25 °C. It describes how many channels can simultaneous support PWM switching at the maximum frequency with 50% duty cycle at different load current level (four levels have been tried 500, 1000, 1500, 2000 mA).

Table 4: STEVAL-IFP029V1 max. switching frequency vs. number of active channels and I_{LOAD} at Tamb = 25 °C

Duty cycle 50%		
I_{LOAD} [mA]	**Number channels**	**Max. PWM frequency [kHz]**
500	1	>250
	2	200
	3	140
	4	100
1000	1	230
	2	100
	3	60
	4	40
1500	1	150
	2	30
	3	10
2000	1	110

5 EMC robustness

EMC robustness has been taken into account using different approaches for the supply voltage line and output lines.

Regarding to the power stage rail, the on-board TVS U8 is used between V_{CC} and ground to clamp the overvoltage in case of surge discharge.

Moreover, the TVS U2 between V_Z pins and V_{CC} rail protects the output pins from the surge pulse.

A third TVS on U9 is necessary to guarantee the board components against surge pulse on V_{DD}.

6 Board layout

The two-layer design allows both a proper heat-sinking capability and noise immunity. The following figures show the component placement, top and bottom side layout.

Figure 3: STEVAL-IFP029V1: component placement

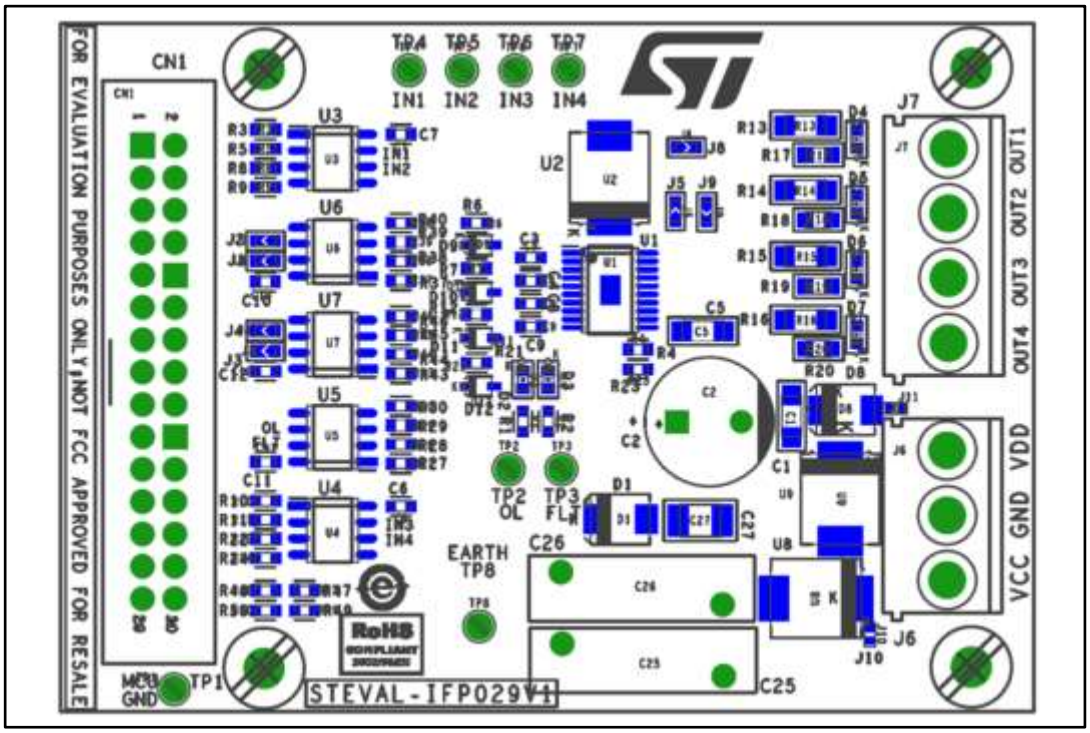


Figure 4: STEVAL-IFP029V1: top side layout

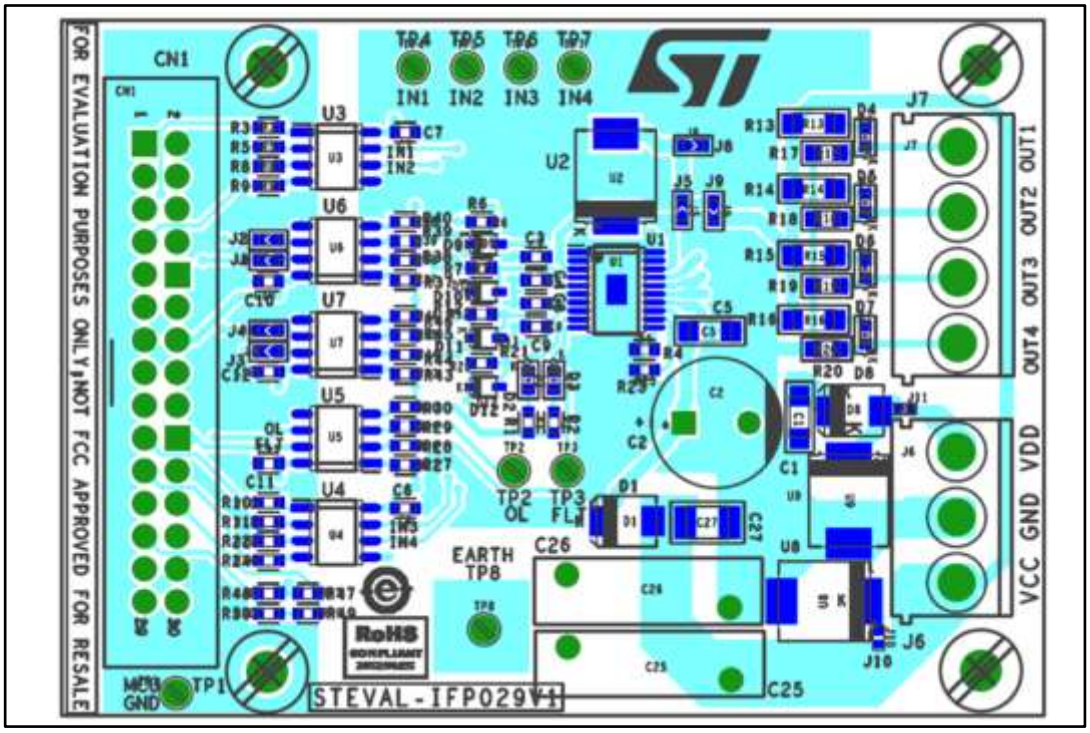
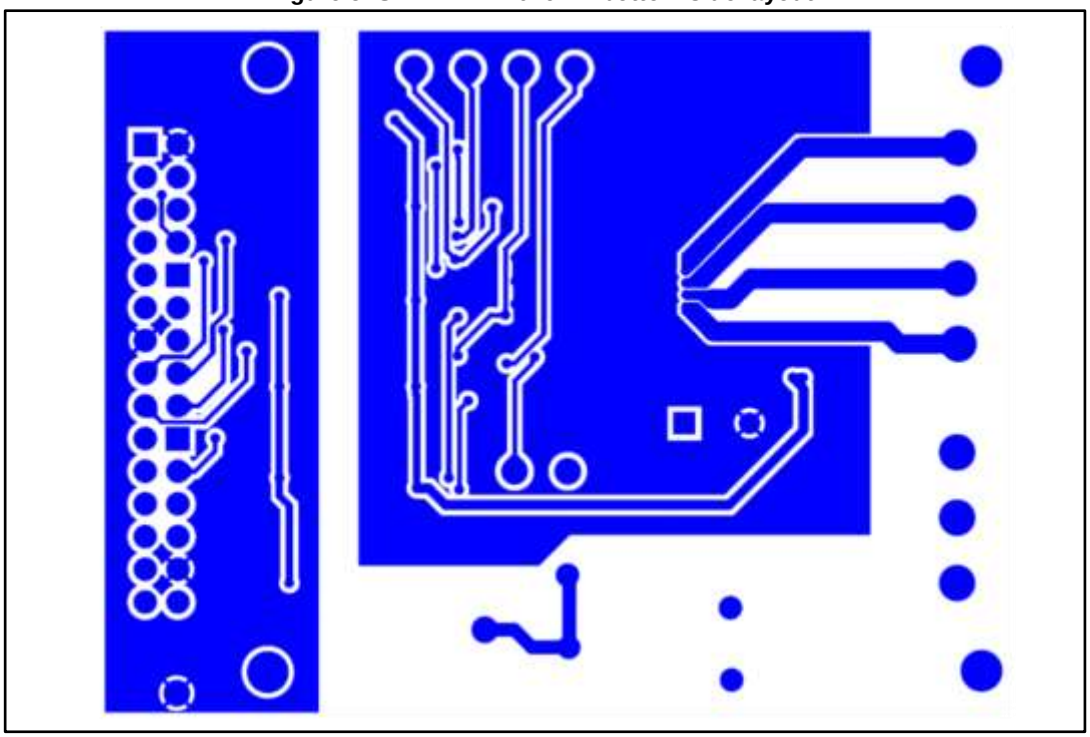


Figure 5: STEVAL-IFP029V1: bottom side layout



7 GUI interface

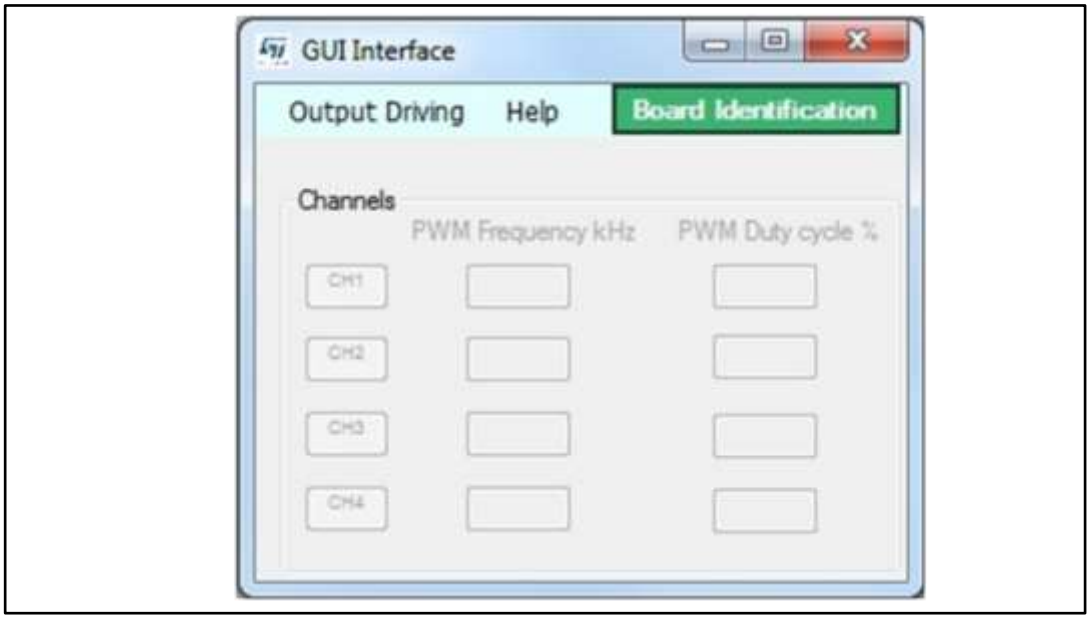
The STSW-IFP029GUI is a graphic user interface allowing an easy control of the STEVAL-IFP029V1 by the STEVAL-PCC009V2 (sold separately). The STSW-IFP029GUI can be downloaded from the *STEVAL-IFP029V1 product folder* and installed without any additional cost on a PC/laptop running Win OS.

The hardware connections are quite simple:

- Connect PC/laptop to the STEVAL-PCC009V2 by a mini-USB cable
- Connect the STEVAL-PCC009V2 to the STEVAL-IFP029V1 by 30-pin flat cable

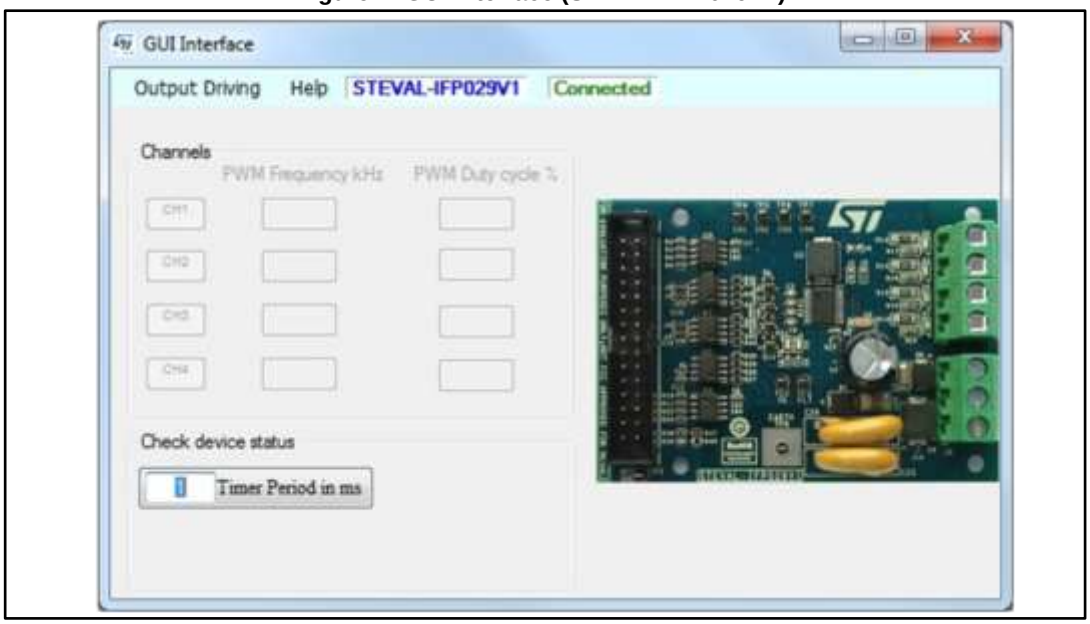
After the hardware connection is completed, the GUI can be launched on the PC/laptop and the following window is displayed.

Figure 6: GUI interface (board identification)



Clicking on “Board identification” the GUI automatically recognizes the STEVAL-IFP029V1.

Figure 7: GUI interface (STEVAL-IFP029V1)



Clicking on the output driving tab, the user can select between the two driving modes:

1. Steady-state driving.
   In this first driving mode, the output can be statically driven ON or OFF.
2. PWM driving.
   In this second driving mode the frequency and duty cycle can be configured while the output can be driven to PWM mode. The values edited in the frequency and duty cycle input text fields are active after clicking on the left buttons of the GUI reporting the channel name (CH_1, CH_2, CH_3 and CH_4). If a channel is activated, then a green box is displayed on the picture of the STEVAL-IFP029V1 in line to the activated channel.

Figure 8: GUI interface (PWM driving)

Note that PWM driving has been implemented using two timers (PWM1 and PWM2) of the microcontroller. The former is used to drive output1 and output2 of the IPS4260L; the latter is used to drive output3 and output4 of the IPS4260L. This implementation introduces a

limitation regarding the parameter settings. In fact, different duty cycles for all outputs can be selected, but the same frequency must be used to drive outpu1 and output 2; the same limitation occurs for the frequency set to drive output3 and output4.

Finally, the GUI is able to report the status of the FLT (collective failure) and OL (open load) pins of the IPS4260L: two small rectangular boxes change their color according to the activation/deactivation (red/green, respectively) of the related open-drain. The status of the chip is periodically checked with time period (in ms) defined in the "Timer Period" input text field.

Figure 9: GUI interface (collective failure/open load)

When the user has completed the test, the following sequence has to be followed:

- Disconnect the power supply from the STEVAL-IFP029V1
- Click on the GUI “Output Driving”-> “Disconnect” menu
- Disconnect the USB cable between PC/laptop and the STEVAL-PCC009V2
- Close the GUI

8 Reference documents

- IPS4260L datasheet
- IEC61000-4-4 European standard
- IEC61000-4-5 European standard
- IEC61000-4-2 European standard
- UM0935

9 Revision history

Table 5: Document revision history

Date	Revision	Changes
05-Oct-2017	1	Initial release.

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