BERTScope™, BERTScope S, BERTScope Si, and BERTScope SPG Signal Integrity Instruments

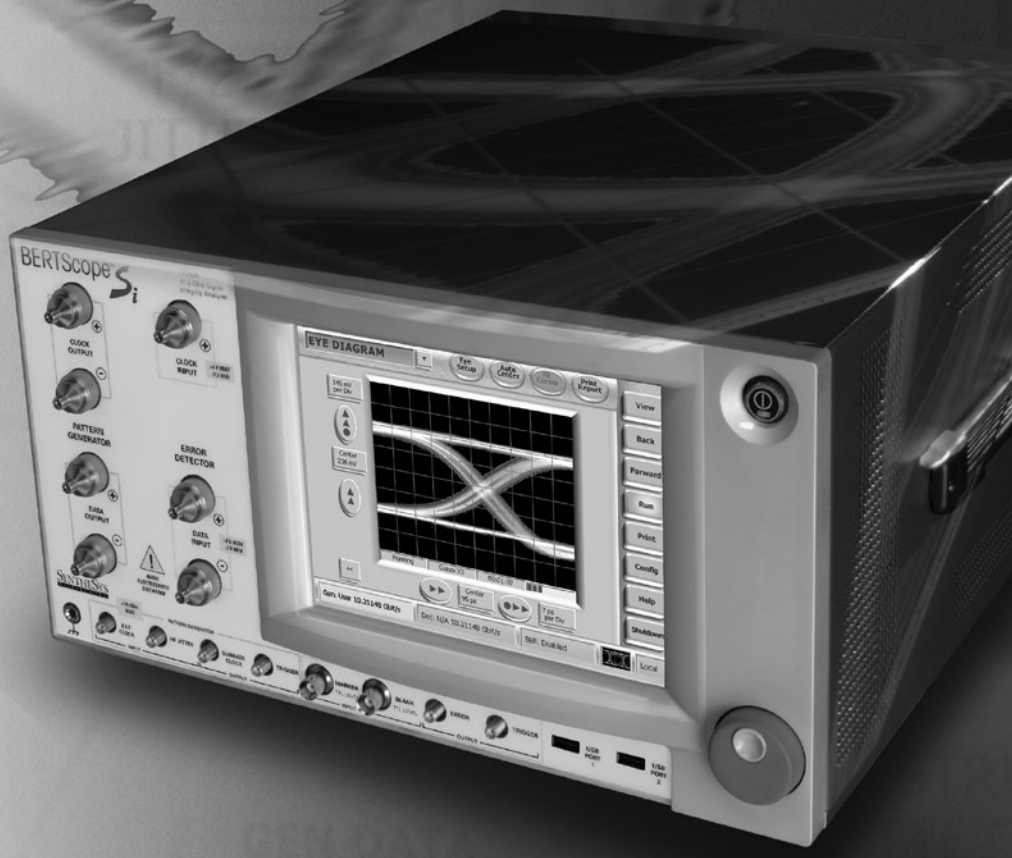
Technical Specifications

Benefits:

- Integrated Signal Integrity Analyzer using the same acquisition circuitry for time, error and jitter domain measurements, to give "same observer" measurements that tie together for faster troubleshooting of your problem devices
- Unique analysis toolkit gives you unrivaled information quality and depth
- 17.5 Gb/s, 12.5 Gb/s, and 7.5 Gb/s (upgradeable) models will cover your needs as your application bit rates increase
- Detailed Jitter Sub-Component analysis - beyond dual-Dirac Random and Deterministic separation

Applications:

- Serial Bus Design
- Semiconductor IC Evaluation
- Jitter Tolerance Compliance Testing
- High Speed Backplane Design
- Optical Transceiver Design and Manufacturing



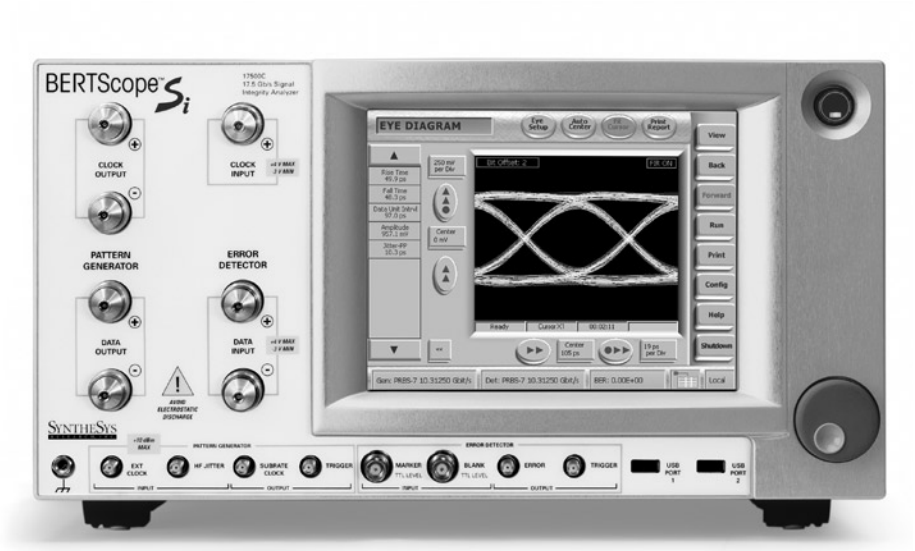
SYNTHESYS RESEARCH, INC.

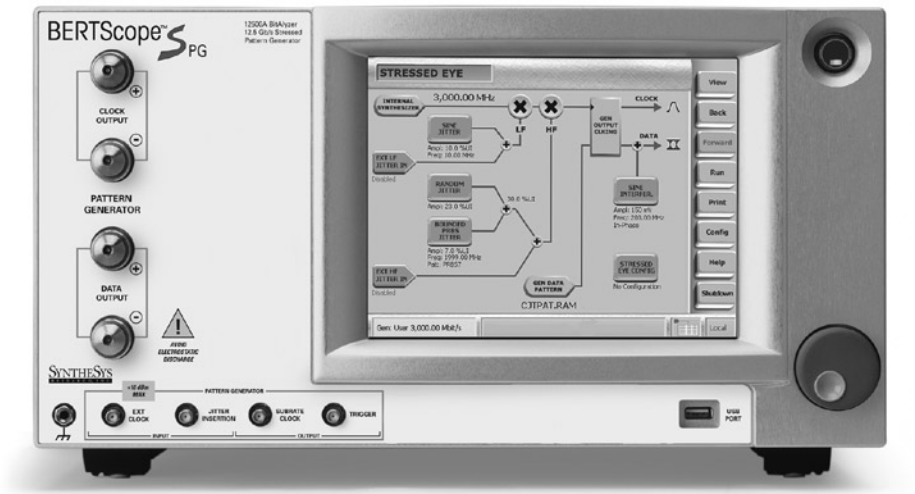
The Vision of a Scope, the Confidence of a BERT, and Clock Recovery you can Count on.

BERTScope, BERTScope S, BERTScope Si, and BERTScope SPG

Technical Specifications

Contents





Model	Applicable Pages
BERTScope 17500A, 12500A, 7500A Signal Integrity Analyzer	Pattern Generator: 3, 4 Error Detector: 9 - 16, 18 General: 19, 20
BERTScope 17500C, 12500B, 7500B Signal Integrity Analyzer with Stress	All
BERTScope SPG 12500B Stress Pattern Generator	Pattern Generator: 3 - 8 User Interface: 12 General: 19 - 20

Pattern Generator
Input/ Output Specifications

Clock and Clock Outputs

Maximum Frequency:	7.5 Gb/s (BSA7500A/B) 12.5 Gb/s (BSA12500A/B) 11.2 Gb/s (BSA17500A/C (output at data rate ÷ 2 above 11.2 Gb/s)
Minimum Frequency:	100 Mb/s (except
Internal Clock	BSA17500A/C) 500 Mb/s (BSA17500A/C)
Phase Noise:	< –90 dBc/Hz @ 10 kHz offset (typical)
Clock Output Divide Ratios:	BERTScope S / Si / SPG models only. See pages 5-6

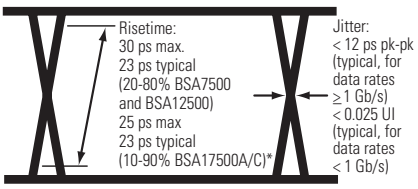
Data and Data Outputs

Date Rate:	0.1 – 7.5 Gb/s (BSA7500A/B) 0.1 – 12.5 Gb/s (BSA12500A/B) 0.5 – 17.5 Gb/s (BSA17500A/C)
Format:	NRZ
Polarity:	Normal or Inverted
Variable Crossover:	25 to 75%
Patterns:	
Hardware Patterns:	
Industry standard Pseudo-Random (PRBS) of the following types: $2^n – 1$ where n = 7, 11, 15, 20, 23, 31	
RAM Patterns:	
User-defined:	
(except BSA17500A/C)	128 bits to 8 Mbits in each of two A/B pages (pages can not be combined)
(BSA17500A/C)	128 bits to 64 Mbits in each of two A/B pages (pages can not be combined)
Library:	Wide variety including SONET/SDH, Fibre Channel-based such as k28.5, CJTPAT; 2^n patterns where n = 3, 4, 5, 6, 7, 9; Mark Density patterns for 2^n where n = 7, 9, 23; and many more.
Error Insertion:	
Length:	1, 2, 4, 8, 16, 32, 64 bit bursts
Frequency:	Single or repetitive

Data/Data, Clock/Clock Amplitudes and Offsets

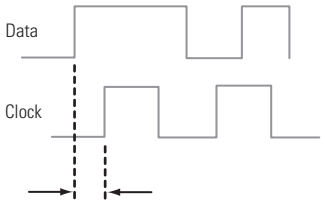
Configuration:	Differential Outputs, each side of pair individually settable for termination, amplitude, offset.
Interface:	DC Coupled, 50 Ω reverse terminated, APC-3.5 connector. Calibration into 75 Ω selectable, other impedances by keypad entry. User-replaceable Planar Crown® adapter allows change to other connector types.
Preset Logic Families:	LVPECL, LVDS, LVTTL, CML, ECL, SCFL
Terminations:	Variable, –2 to +2V. Pre-sets: +1.5, +1.3, +1, 0, –2 V, AC-Coupled
Allowable Amplitudes, Terminations, and Offsets:	See Figures 1 and 2

Data/Data, Clock/Clock Waveform Performance



*measured with a 50 GHz or greater sampling oscillocope

Clock/Data Delay



Range:

Up to 1.1 GHz	30 ns
Above 1.1 GHz	3 ns

(Greater than 1 bit period in all cases)

Resolution: 100 fs

Self-Calibration:

Supported – at time of measurement, when temperature or bit rate are changed, instrument will recommend a self calibration. Operation takes less than 10 seconds.

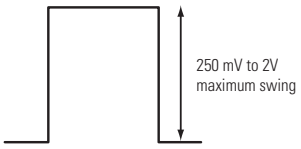


Figure 1. Amplitude range.

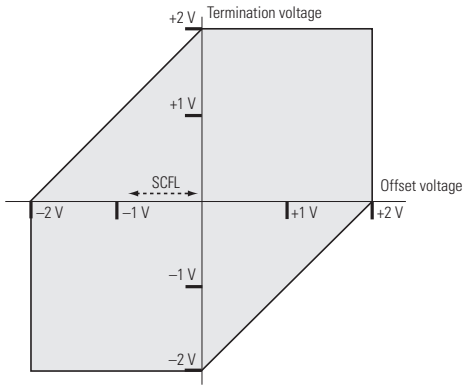
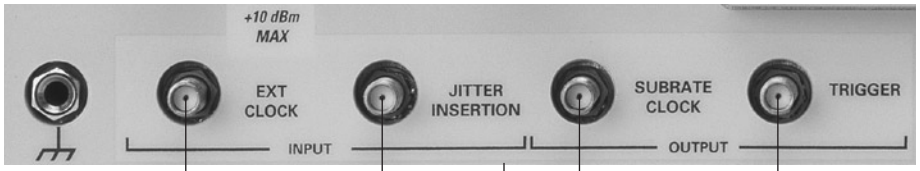


Figure 2. Allowable combinations of termination and offset. Amplitude swings between 0.25 and 2 V allowed; should fit inside shaded area of graph. For example, SCFL uses a 0 V termination, and operates between approximately 0 and –0.9 V; as shown with dotted arrow, it falls within the operating range.

Pattern Generator Ancillary Connections

Front Panel Pattern Generator Connections



External Clock Input

Allows use of an external clock source to clock the BERTScope.
Models equipped with stress are able to add impairments to incoming clock, including when external signal has spread spectrum clocking (SSC) in excess of 5000 ppm imposed on it. See Page 5 for more details.

Frequency Range:	0.1 to 7.5 GHz (BSA 7500A/B) 0.1 to 12.5 GHz (BSA12500A/B) 0.5 to 17.5 GHz (BSA17500A/C)
Nominal Power:	900 mV p-p (+3 dBm)
Maximum Power:	2.0 V p-p (+10 dBm)
Return Loss:	Better than –6 dB
Interface:	50 Ω SMA female, DC coupled into selectable termination voltage.

Trigger Output

Provides a pulse trigger to external test equipment. It has two modes:
1. Divided Clock Mode: Pulses at 1/256th of the clock rate
2. Pattern Mode: Pulse at a programmable position in the pattern (PRBS), or fixed location (RAM patterns)

Stress modulation added on models so equipped, when enabled

Minimum Pulse Width:	128 Clock Periods (Mode 1) 512 Clock Periods (Mode 2)
Transition Time:	< 500 ps
Jitter (p-p, data to trigger)**:**	< 10 ps, typical (BSA17500A/C)
Output Levels:	> 300 mV -p-p, center at 650 mV
Interface:	50 Ω SMA female,

Jitter Insertion (BERTScope S/Si/SPG models)

One of two jitter insertion inputs. Can be used to insert SJ, RJ, BUJ if desired.

Frequency Range:	DC to 1.0 GHz
Jitter Amplitude Range:	Up to 0.5 UI (max.)
Input Voltage Range:	0 - 2 V p-p (+10 dBm) for normal operation 6.3 V p-p (+20 dBm) Max. non-destruct input
Interface:	SMA female 50 Ω, DC coupled into 0 V

Sub-Rate Clock Output

BERTScope model has clock divided by 4.
BERTScope S/Si/SPG models have additional capabilities. See page 5, 6.

Frequency Range:	0.125 to 3.125 GHz (12.5 GHz BERTScope S/Si/SPG)
Amplitude Range:	1 V p-p, nominal, centered around 0 V
Transition Time:	< 500 ps
Interface:	SMA female, 50 Ω, DC coupled into 0 V

Rear Panel Pattern Generator Connections

Pattern Start Input

For users wanting to synchronize patterns of multiple data streams from multiple instruments simultaneously.

Logic Levels:	LVTTL (< 0.5 V Lo, > 2.5 V hi)
Threshold:	+1.2 V typical
Max Non-distructible Input range:	-0.5 V to +5.0 V
Minimum Pulse Width:	128 serial clock periods
Maximum Repetition Rate:	512 serial clock periods
Interface:	SMA female, > 1 kΩ impedance into 0 V

Low Frequency Jitter Input

(BERTScope S/Si/SPG models)
Allows use of external low frequency sinusoidal jitter source to modulate the stressed pattern generator output.

Frequency Range:	DC to 100 MHz
Jitter Amplitude Range:	Up to 1 ns
Input Voltage Range:	0 - 2 V p-p (+10 dBm) for normal operation 6.3 V p-p (+20 dBm) Max. non-destruct input
Interface:	SMA female 50 Ω, DC coupled into 0 V

Reference Input (Option XSSC and BSA17500A/C)

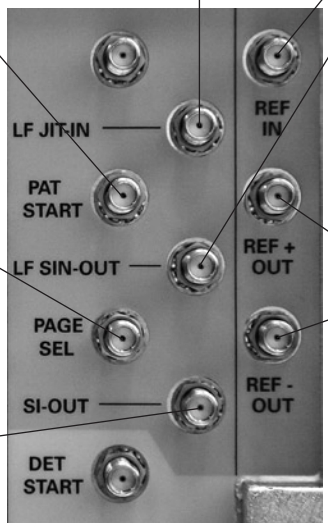
To lock the BERTScope to an external frequency reference from of another piece of equipment.

Frequency:	10, 100, 106.25, 133.33, 156.25, 166.67, or 200 MHz
Amplitude:	0.325 to 1.25 Vp-p (-6 to +6 dBm)
Interface:	50 Ω SMA female, AC coupled

Page Select Input

In A-B Page Select Mode, allows external control of pattern. Logic 1 applied to input switches to Pattern B at the next completion of Pattern A.

Logic Levels:	LVTTL (< 0.5 V Lo, > 2.5 V hi)
Threshold:	+1.2 V typical
Max Non-distructible Input range:	-0.5 V to +5.0 V
Minimum Pulse Width:	1 pattern length
Interface:	SMA female, > 1 kΩ impedance into 0 V



Low Frequency Sinusoidal Jitter Output (BERTScope S/Si/SPG models)

To allow phasing of two BERTScopes together, in-phase or anti-phase.

Frequency:	As set for internal SJ from GUI
Amplitude:	2 V p-p, centered at 0 V
Interface:	SMA female

Reference Output (Option XSSC and BSA17500A/C)

Provides a frequency reference for other instruments to lock to.

Configuration:	Differential
Frequency:	10, 100, 106.25, 133.33, 156.25, 166.67, or 200 MHz
Amplitude:	1 V p-p (+4 dBm) nominal, each output, (2 V p-p differential)
Interface:	50 Ω SMA female, AC coupled

Sinusoidal Interference Output

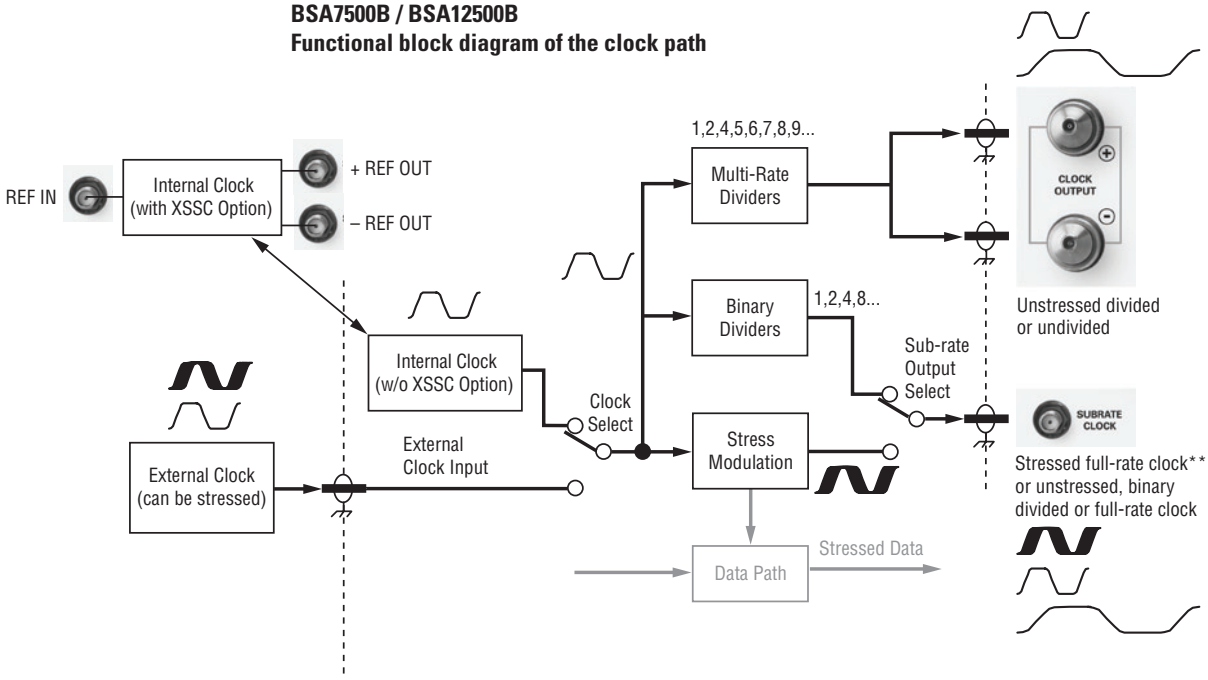
(BERTScope S/Si/SPG models)
SI output from internal generator. Can be used to apply SI after external ISI channel.

Frequency Range:	0.1 - 2.5 GHz
Ouput Voltage:	0 - 3 V p-p
Interface:	50 Ω SMA female , AC coupled

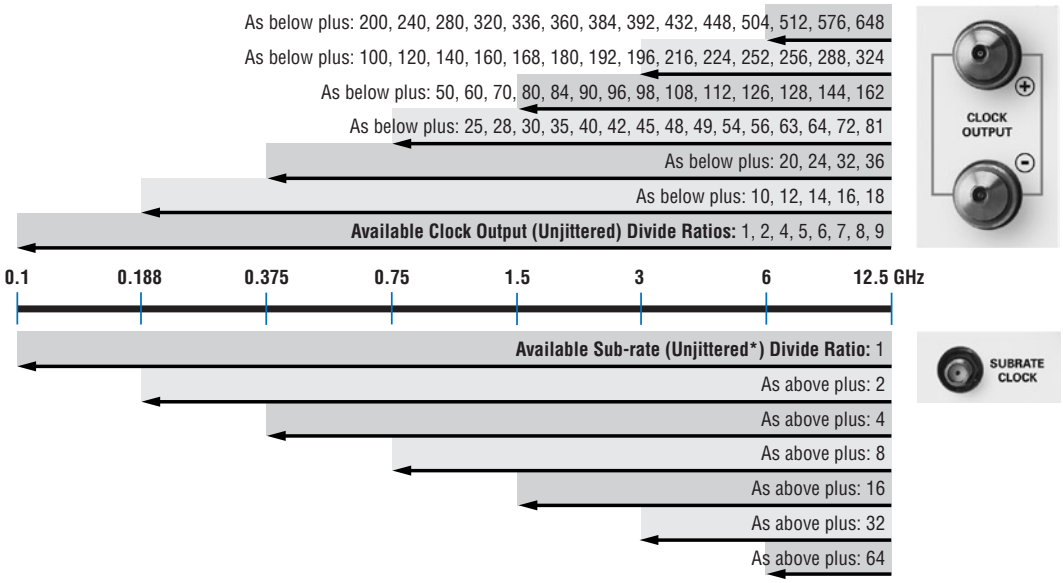
Clocking Diagram For Models With Stress Capability

BERTScope S/SPG

BSA7500B / BSA12500B
Functional block diagram of the clock path



Available divide ratios from clock-related output, by bit rate, using the internal clock, BSA7500A/B and BSA12500A/B†



* This output can also provide a full-rate jittered clock.

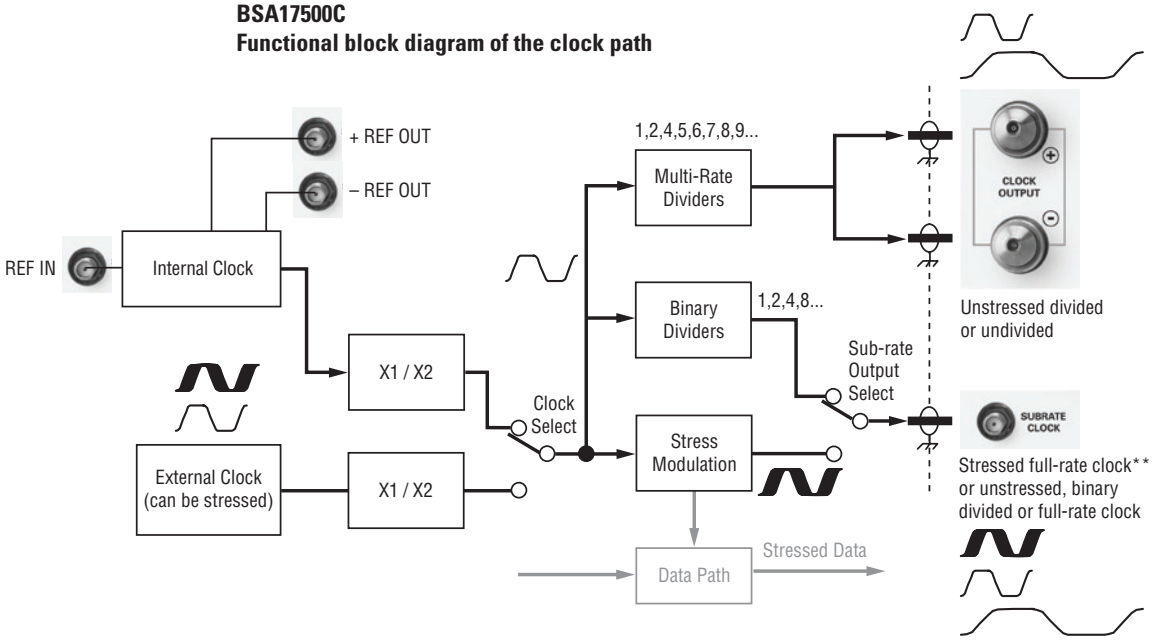
† All listed ratios available for an external clock input over entire bit-rate range, limitations for internal clock only. Minimum specified frequency of the clock output is 100 MHz. Operation below this rate will be uncalibrated.

** Stress may be added to an external clock on appropriate models. Stress operating range is from 1.45 to 11.2 Gb/s. External clock must have a duty cycle of 50% ±2%.

Clocking Diagram For Models With Stress Capability

BERTScope Si

BSA17500C
Functional block diagram of the clock path



Available Multi-Rate and Sub Rate divider ratios for main clock output, BSA17500A / BSA17500C models

The BS17500 models use an internal Double Data Rate (DDR) architecture to operate at data rates ≥ 11.2 Gb/s. When operating at 11.2 Gb/s or higher data rate, the clock output will be ½ the data rate.

External clock can be specified to be either full or half data rate. When full rate is selected, the pattern generator will operate in DDR mode when the input clock frequency is 11.2 GHz or higher.

These ratios apply to operation from internal clock only. External clock will be output at ½ rate when half rate is selected, or when full rate is selected and clock rate is ≥ 11.2 GHz.

The minimum data rate specified for the main Clock Output is 500 Mb/s. Output will be uncalibrated when operated at divided rates lower than 500 Mb/s.

Clock Rate (Gb/s)	Ratios for Main Clock Out	Ratios for Subrate Clock Out*
500 – 750 Mb/s	1, 2, 4, 5, 6, 7, 8, 9, 10, 12, 14, 16, 18, 20, 24, 32, 36	1, 2, 4
0.75 – 1.5 Gb/s	1, 2, 4, 5, 6, 7, 8, 9, 10, 12, 14, 16, 18, 20, 24, 25, 28, 30, 32, 35, 36, 40, 42, 45, 48, 54, 56, 64, 72, 81	1, 2, 4, 8
1.5 – 3 Gb/s	1, 2, 4, 5, 6, 7, 8, 9, 10, 12, 14, 16, 18, 20, 24, 30, 32, 32, 35, 36, 36, 40, 42, 45, 48, 50, 54, 56, 60, 64, 70, 72, 80, 81, 84, 90, 98, 108, 112, 126, 128, 144, 162,	1, 2, 4, 8, 16
3 – 6 Gb/s	1, 2, 4, 5, 6, 7, 8, 9, 10, 12, 14, 16, 18, 20, 24, 30, 32, 32, 35, 36, 36, 40, 42, 45, 48, 50, 54, 56, 60, 64, 70, 72, 80, 81, 84, 90, 98, 100, 108, 112, 120, 126, 128, 140, 144, 160, 162, 168, 180, 192, 196, 216, 224, 252, 256, 288, 324,	1, 2, 4, 8, 16, 32
6 – 11.2 Gb/s	1, 2, 4, 5, 6, 7, 8, 9, 10, 12, 14, 16, 18, 20, 24, 30, 32, 32, 35, 36, 36, 40, 42, 45, 48, 50, 54, 56, 60, 64, 70, 72, 80, 81, 84, 90, 98, 108, 112, 126, 128, 140, 144, 144, 160, 162, 162, 168, 180, 192, 196, 200, 216, 224, 240, 252, 256, 280, 288, 320, 324, 360, 384, 392, 432, 448, 504, 512, 576, 648,	1, 2, 4, 8, 16, 32, 64
11.2 – 12 Gb/s	2, 4, 8, 10, 12, 14, 16, 18, 20, 24, 28, 32, 36, 40, 48, 60, 64, 64, 70, 72, 72, 80, 84, 90, 96, 100, 108, 112, 120, 128, 140, 144, 160, 162, 168, 180, 196, 200, 216, 224, 240, 252, 256, 280, 288, 320, 324, 336, 360, 384, 392, 432, 448, 504, 512, 576, 648	2, 4, 8, 16, 32, 64
12 – 17.5 Gb/s	2, 4, 8, 10, 12, 14, 16, 18, 20, 24, 28, 32, 36, 40, 48, 60, 64, 64, 70, 72, 72, 80, 84, 90, 96, 100, 108, 112, 120, 128, 140, 144, 160, 162, 168, 180, 196, 216, 224, 252, 256, 280, 288, 288, 320, 324, 324, 336, 360, 384, 392, 400, 432, 448, 480, 504, 512, 560, 576, 640, 648, 720, 768, 784, 864, 896, 1008, 1024, 1152, 1296	2, 4, 8, 16, 32, 64, 128

* Subrate clock connector can also output a full rate stressed clock up to 11.2 Gb/s, or half rate stressed clock at rates ≥ 11.2 Gb/s.

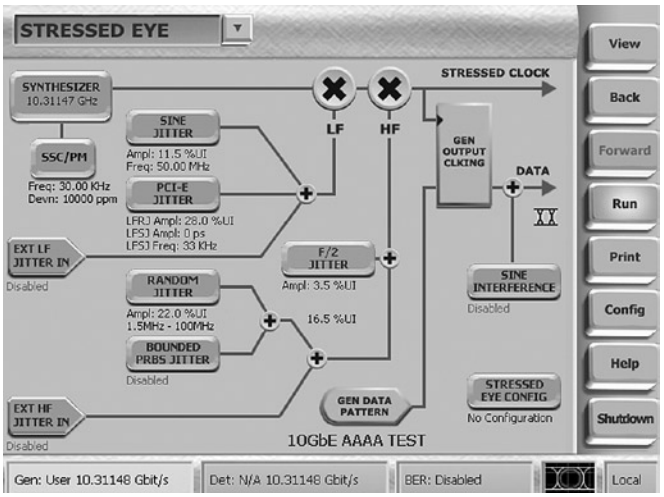
Pattern Generator Stressed Eye

BERTScope S/Si/SPG

- Flexible, integrated stressed eye impairment addition to the internal or an external clock
- Easy set-up, with complexity hidden from the user with no loss of flexibility
- Verify compliance to multiple standards using the BERTScope and external ISI filters. Standards such as:
  - OIF CEI
  - 6 Gb SATA
  - PCI-Express®
  - XFI
  - USB3.0
  - SONET
  - SAS 2
  - XAUI
- Sinusoidal interference may be inserted in phase or in anti-phase, or sent externally to be summed after an external ISI reference channel.
- Sinusoidal jitter may be locked between two BERTScopes in phase or anti-phase, as required by OIF CEI

Flexible External Jitter Interfaces:

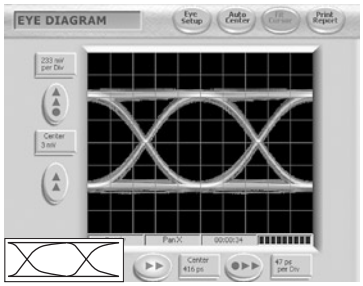
- Front Panel External High Frequency Jitter Input Connector – Jitter from DC to 1.0 GHz up to 0.5 UI (max.) may be added, of any type that keeps with amplitude and frequency boundaries
- Rear Panel External SJ Low Frequency Jitter Input Connector – Jitter from DC to 100 MHz up to 1ns (max) may be added
- Rear Panel SJ Output
- Sinusoidal Interference Output rear panel connector



Notes: Specified for data rates from 1.45 Gb/s to 11.2 Gb/s (BSA12500B), to 17.5 Gb/s (BSA17500CSi). Usable with limited performance to 622 Mb/s. Internal RJ, BUJ, and external high frequency jitter input limited to 0.5 UI, combined, further limited to 0.25 UI each when both are enabled. Rear panel low frequency jitter input can be used to impose additional jitter; internal and external jitter sum total cannot exceed jitter magnitude limits given for SJ below.

Amplitude & ISI Impairments

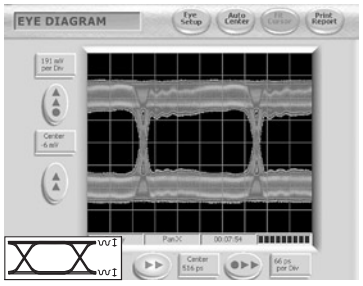
ISI



Add externally: For example long coax cable length, or Bessel-Thompson 4th Order Filter with –3 dB point at 0.75 of Bit Rate etc.

For applications requiring circuit board dispersion, the BERTScope differential ISI accessory may be used.

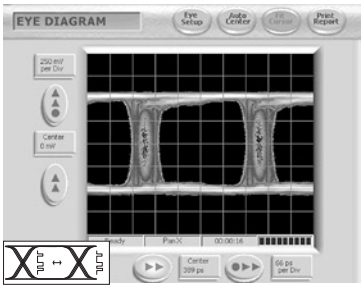
Sinusoidal Interference



- 100 MHz to 2.5 GHz
- Adjustable in 100 kHz steps
- Adjustable from 0 to 400 mV
- Common mode or differential
- Available from rear panel 50 Ω SMA connector, single-ended with data amplitude from 0 to 3 V adjustable from GUI, same frequency range and step size as internal adjustment

Jitter Impairments

Bounded Uncorrelated Jitter

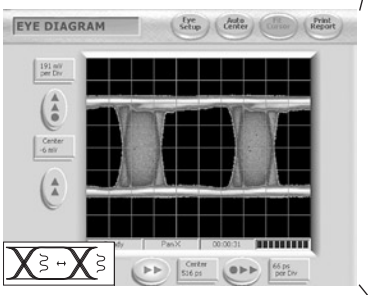


- Internal PRBS Generator PN-7
- Variable up to 0.5 UI
- 100 Mb/s to 2.0 Gb/s
- Band limited by selected filters

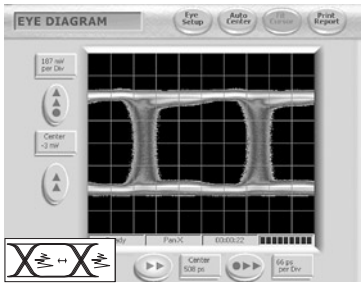
– see table below:

BUJ Rate	Filter (MHz)
100 to 499	25
500 to 999	50
1,000 to 1,999	100
2,000	200

Sinusoidal Jitter



Random Jitter



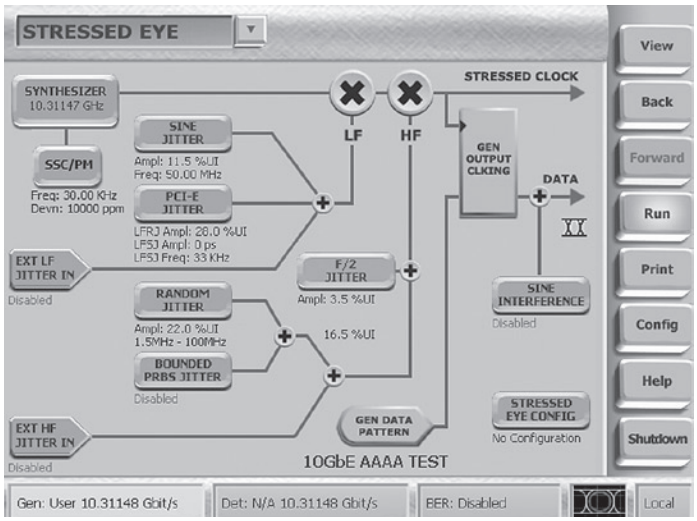
- Variable up to 0.5 UI
- Band limited 10 MHz to 1 GHz
- Crest factor of 16 (Gaussian to at least 8 standard deviation or ~1x10^{-16} probability)

Data Rate	Internal SJ Frequency Range	
	1kHz to 10 MHz*	10 MHz to 100 MHz
10.3125 Gb/s	10.3 UI	2.1 UI
9.9545 Gb/s	10.0 UI	2.0 UI
8.5 Gb/s	8.5 UI	1.7 UI
6.25 Gb/s	6.3 UI	1.3 UI
6 Gb/s	6.0 UI	1.2 UI
5 Gb/s	5.0 UI	1.0 UI
4.25 Gb/s	4.3 UI	0.9 UI
3.125 Gb/s	3.1 UI	0.6 UI
3 Gb/s	3.0 UI	0.6 UI
2.5 Gb/s	2.5 UI	0.5 UI
2.4883 Gb/s	2.5 UI	0.5 UI
2.125 Gb/s	2.1 UI	0.4 UI
1.5 Gb/s	1.5 UI	0.3 UI

SJ adjustable from 0 to levels greater than or equal to range in table.

* For models equipped with PCIe stress source option, this column is the maximum total stress amplitude of the LF SJ + LF RJ levels.

Additional Stress Options



Enhanced Spread Spectrum Clock Option
(Standard in BSA Si models Option XSSC, available in BERTScope B models)

Adds a modulator directly to the synthesizer clock output – modulation affects main and subrate clock output (regardless of the state of sub-rate output select), Data Output, and Trigger Output.

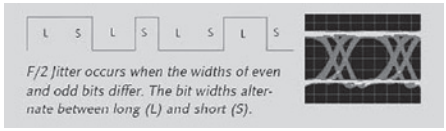
Modes:	SSC or Phase Modulation (sinusoidal)
Clock Frequency Range:	Full range of BERTScope clock synthesizer
SSC Waveshape:	Triangle or Sine
SSC Frequency Range:	20 kHz to 40 kHz
SSC Modulation Range:	12,500 PPM at 6 Gb/s 6,200 PPM at 12 Gb/s 6,000 PPM at 12.5 Gb/s 6,000 PPM at 17.5 Gb/s (BSA17500C) See plot below for range at lower clock rates.
SSC Modulation Resolution:	1 PPM
SSC Modulation Type:	Down Spread, Center Spread, Up Spread
PM Frequency Range:	10 Hz – 160 kHz
PM Frequency Resolution:	1 Hz
PM Modulation Range:	For modulation frequency 10 Hz – 2 kHz:

Clock Rate (Gb/s)	Maximum Modulation (UI)
6 to 12.5 6 to 17.5 (BSA17500C)	6000
3 to 6	3000
1.5 to 3	1500
0.75 to 1.5	750
375 to 750 Mb/s	375
187 to 375 Mb/s	187.5
100 to 187 Mb/s	93.75

Reduced for modulation frequencies > 2 kHz. See plot below.

F/2 Jitter Generation Option
(Option -F2 in BSA B and CSi models)

F/2 or subrate jitter is found in high data rate systems which multiplex up 2 or more lower data rate streams. The jitter results for lack of symmetry in the multiplexing clock, giving all of the even bits different pulse width than the odd bits. Unlike conventional DCD, F/2 jitter is independent of the logic state of the bit. F/2 Jitter is part of the stress recipe used in testing compliance to some of the newer standards such as 802.3ap (10 Gb backplane Ethernet).



F/2 Jitter occurs when the widths of even and odd bits differ. The bit widths alternate between long (L) and short (S).

Supported Data Rates:	8.0 and 10.3125 Gb/s
Modulation Range:	0 - 5.0% UI

Extended Stress Generation Option
(Standard in BSA -PCIE models
Option -XS in BSA Si models)

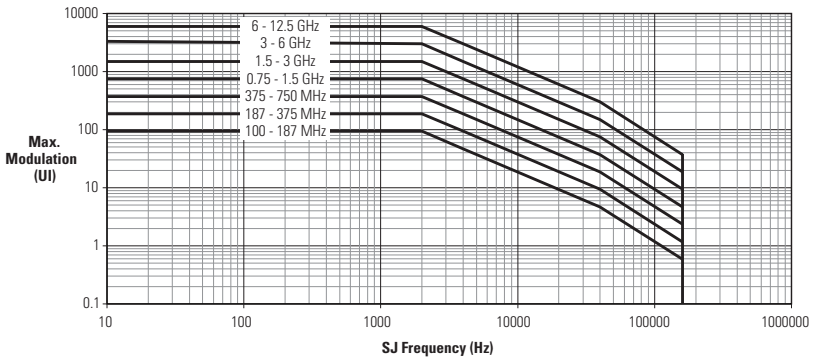
This option adds two additional stress generators required for compliance testing receivers to PCIe G2 specifications, internal to the BERTScope.

Clock Frequency Range:	Up to 11.2 Gb/s
LFRJ Modulation Range:	0 - 1.1 ns, sum of LFRJ + 1 kHz - 10 MHz SJ. See table on page 7 for range in UI equivalents.
LFRJ Frequency Range:	Band limited to 10 kHz – 1.5 MHz, with roll off to PCIe G2 specifications
LFSJ Modulation Range:	0 – 368 ps @ 5 Gb/s
LFSJ Frequency Range:	1 – 100 kHz

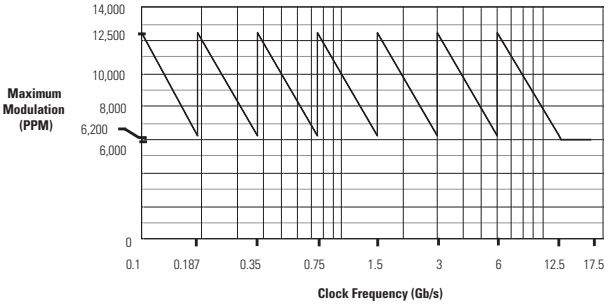
The Extended Stress option also adds selectable bandwidth limiting to the normal, broad band RJ generator:

RJ Frequency, Normal Mode:	Band limited to 10 MHz – 1 GHz
RJ Frequency, PCIE Mode:	Band limited to 1.5 MHz – 100 MHz with roll off to PCIe G2 specifications

Phase Modulation Range



Maximum SSC Modulation



Error Detector

Clock and Data Inputs

Clock Input

Configuration:	Single-ended
Maximum Frequency:	17.5 Gb/s (BSA 17500A/C) 12.5 Gb/s (BSA12500A/B) 7.5 Gb/s (BSA 7500A/B)
Minimum Frequency:	100 Mb/s
Data Sampling Edge:	Rising

Data/$\overline{\text{Data}}$ and Clock Interfaces

Connector:	APC-3.5 Planar Crown®
Impedance:	50 Ω
Threshold Voltage:	-2 to +3.5 V
Threshold Presets:	LVPECL, LVDS, LVTTL, CML, ECL, SCFL.
Terminations:	Variable, –2 V to +3 V Pre-sets: +1.5, +1.3, +1, 0, –2 V, AC-Coupled
Maximum Non-distruct Input:	-3V pk, +4 V pk, applied to any connector

Data and $\overline{\text{Data}}$ Inputs

Configuration:	Differencial
Format:	NRZ
Polarity:	Normal or Inverted
Threshold Alignment:	Can Auto-Align to differential crossing point
Sensitivity:	
Single-Ended	100 mV p-p (typical)
Differential:	50 mV p-p (typical)
Maximum input Signal Swing:	2 V p-p
Intrinsic Transition Time:	16 ps typical, 1/90%, single ended (equivalent to > 20 GHz detector bandwidth). Measured at input, ECL levels.

Patterns:

Hardware Patterns:

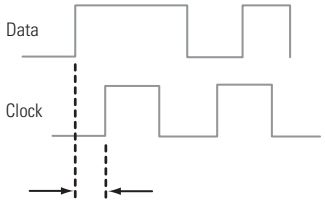
Industry standard Pseudo-Random (PRBS) of the following types: $2^n - 1$ where n = 7, 11, 15, 20, 23, 31

RAM Patterns:

User-defined:	128 bits to 8 Mbits (128 bits to 64 Mbits in BSA17500A/C) 128-bit increments
Library:	Wide variety including SONET/SDH, Fibre Channel-based such as k28.5, CJTPAT; 2^n patterns where n = 3, 4, 5, 6, 7, 9; Mark Density patterns for 2^n where n = 7, 9, 23; and many more.

RAM Pattern Capture:	Capture incoming data up to 8 Mbit in length (128 Mbit in BSA17500A/C). Edit captured data, send to Pattern Generator, Error Detector or both.
Capture Modes:	
Capture by Length:	1 to 65,536 words (BSA7500, BSA12500), 1 to 1,000,000 words (BSA17500), 1 word default. Words 128 bit in length.
Capture by Triggers:	Captures when "Detector Start" on rear panel goes high, to maximum allowable length or until input goes low.
Capture by Length from Trigger:	Capture by length initiated from Detector Start input, to pre-specified length.
Synchronization:	User-specified number of
Auto-Resync:	128 bit words containing 1 or more errors per word initiates a re-sync attempt.
Manual:	User initiates re-sync
Pattern Matching:	
Grab 'n' Go	Error Detector captures specified pattern length and compares next instances to find match. (Fast method, but susceptible to ignoring logical errors.)
Shift-to-Sync	Error Detector compares incoming pattern with reference RAM pattern, looks for match, if none found, shifts pattern by one bit and compares again. (Slower but most accurate method.)
Error Detector Basic Measurements:	BER, Bits Received, Re-Syncs, Measured Pattern Generator and Error Detector clock frequencies

Clock/Data Delay



Range:	
Up to 1.1 GHz	30 ns
Above 1.1 GHz	3 ns

(Greater than 1 bit period in all cases)

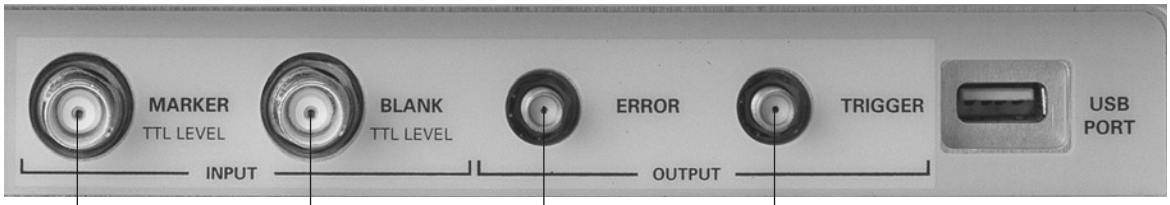
Resolution: 100 fs

Self-Calibration:

Supported – at time of measurement, when temperature or bit rate are changed, instrument will recommend a self calibration. Operation takes less than 10 seconds.

Error Detector Ancillary Connections

Front Panel Error Detector Connections



Error Correlation Marker Input

(Error Analysis)

Allows an external signal to provide a time-tagged marker to be placed in the error data set.

Logic Family:	LVTTL (< 0.5 V Lo, > 2.5 V hi)
Threshold:	+1.2 V
Minimum Pulse Width:	128 Clock Periods
Maximum Repetition Rate:	512 serial clock periods
Maximum Frequency:	< 4000 markers/sec recommended
Interface:	BNC female, > 1 KΩ impedence into 0 V

Trigger Output

Provides a pulse trigger to external test equipment. It has two modes:

1. Divided Clock Mode: Pulses at 1/256th of the clock rate
2. Pattern Mode: Pulse at a programmable position in the pattern (PRBS), or fixed location (RAM patterns)

Minimum Pulse Width:	128 Clock Periods (Mode 1) 512 Clock Periods (Mode 2)
Transition Time:	< 500 ps
Jitter, Data to Jitter:	< 10 ps typical, BSA17500A/C
Output Levels:	> 300 mV amplitude, 650 mV offset
Interface:	50 Ω SMA female

Blank Input

Useful for re-circulating loop fiber experiments or during channel training sequences. Causes errors to be ignored when active. Bit count, error count & BER not counted. No re-sync occurs when counting re-enabled.

Logic Family:	LVTTL (< 0.5 V Lo, > 2.5 V hi)
Threshold:	+1.2 V
Minimum Pulse Width:	128 Clock Periods
Maximum Repetition Rate:	512 serial clock periods
Interface:	BNC female, > 1 KΩ impedence into 0 V

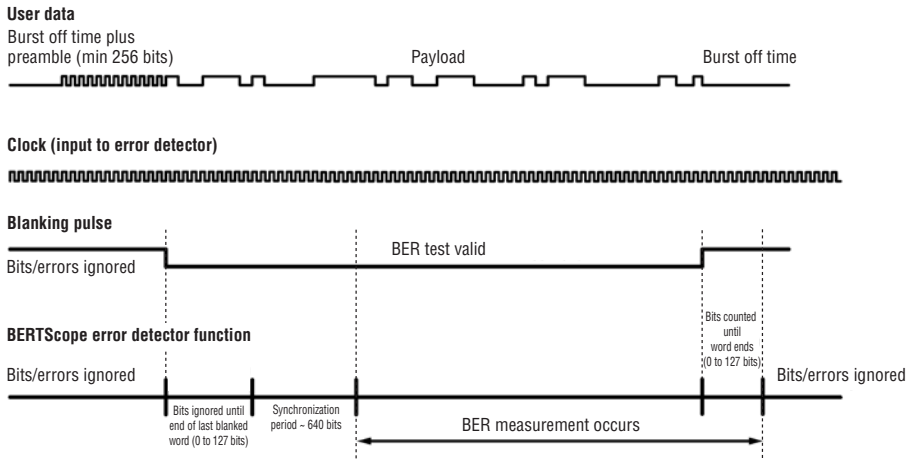
Error Output

Provides a pulse when an error is detected. Useful for triggering an alarm while doing long-term monitoring, etc.

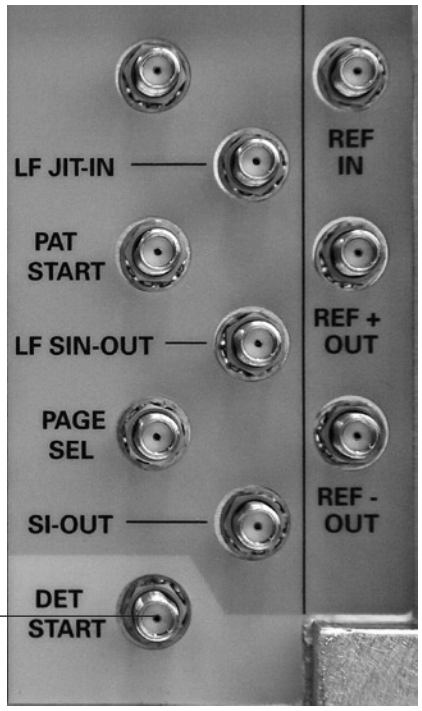
Minimum Pulse Width:	128 Clock Periods
Transition Time:	< 500 ps
Output Levels:	1000 mV nominal (0 V to 1 V low-high)
Interface:	SMA female

BERTScope word size is 128 bits. An example timing diagram is shown here for a PRBS payload. Counting of bits will not start until a 128 bit word boundary occurs, meaning that after the blanking pulse transitions, up to 127 bits may pass before synchronization begins. For a PRBS, synchronization typically takes 5 words, or 640 bits. Similarly, bit measurement will continue for up to 127 bits after the blanking signal transitions again. RAM-based patterns take longer to synchronize.

BERTScope burst analysis timing



Rear Panel Error Detector Connections



Detector Start Input

Used to trigger the acquisition of incoming data into the Error Detector reference pattern memory. High level starts capture.

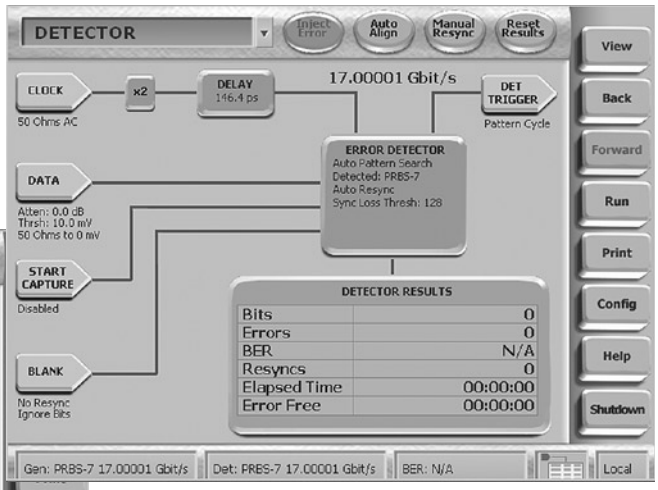
Amplitude:	LVTTL (< 0.5 V Lo, > 2.5 V hi)
Threshold:	+1.2 V
Minimum Pulse Width:	128 serial clock periods
Maximum Repetition Rate:	512 serial clock periods
Interface:	SMA female, > 1 kΩ impedance into 0 V

(Not present for BERTScope SPG)

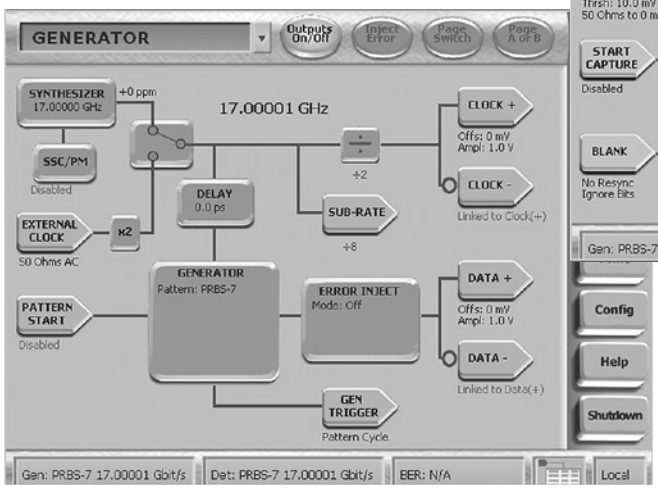
User Interfaces

Taking Usability to New Heights

- Easy navigation
- Logical layout and operation
- Multiple ways of moving between screens
- Relevant information right where you need it
- Color-coding to alert you to the presence of non-standard conditions

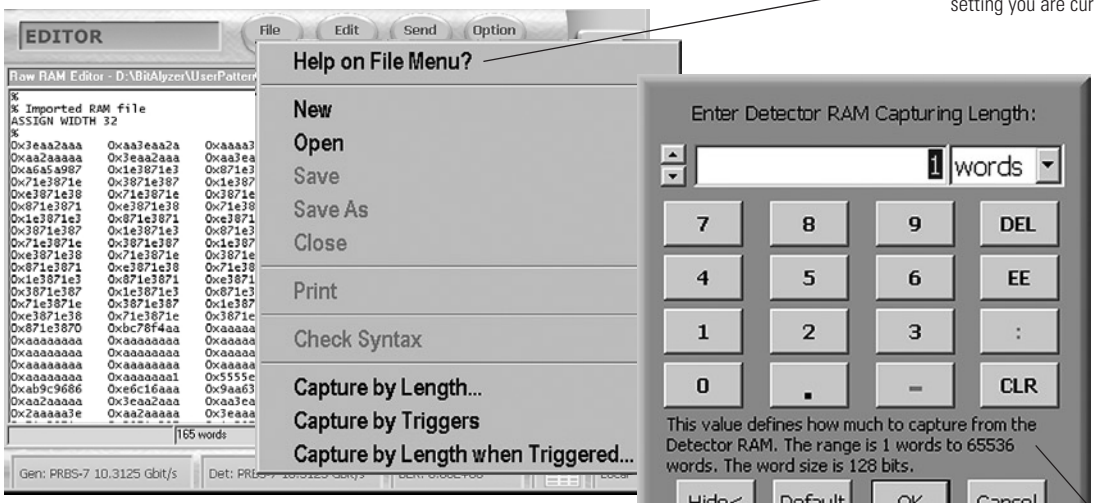


Error Detector Set-Up Screen



Pattern Generator Set-Up Screen

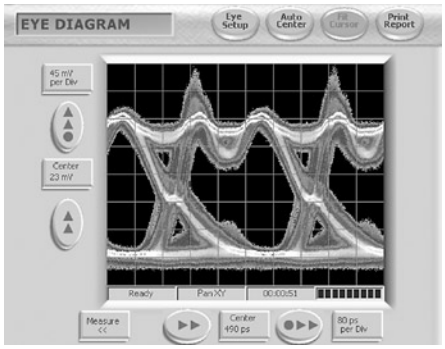
Pull down menus include links to context sensitive help which quickly gives you more information on the setting you are currently focused on.

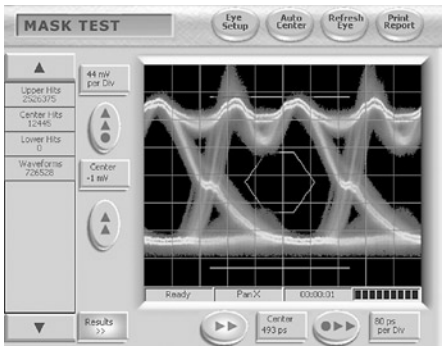


Editor Screen

- Used for pattern editing of standard and AB Page Select patterns, also mask editing
- Views in Binary, Decimal or Hexadecimal
- Support for variable assignments, repeat loops, seeding of PRBS patterns
- Capture and editing of incoming data - for example, to make a repeating pattern out of real-world traffic
  - Capture is available by trigger, by length or by length following a trigger
  - Capture is by number or words, 1 word is 128 bits. For example, a PRBS-7 (127 bits long) would be captured as 127 words, and would have overall length of 16,256 bits.

A numeric input keyboard appears when setting numeric parameters. For reference, the valid range of input values is listed below the keys. The front panel knob can also be used to increment or decrement the value when the data entry screen is active.





BERTScope Built-In Parametric Measurements

All BERTScopes come with Eye Diagrams and Mask Test capabilities as standard, along with Error Analysis.

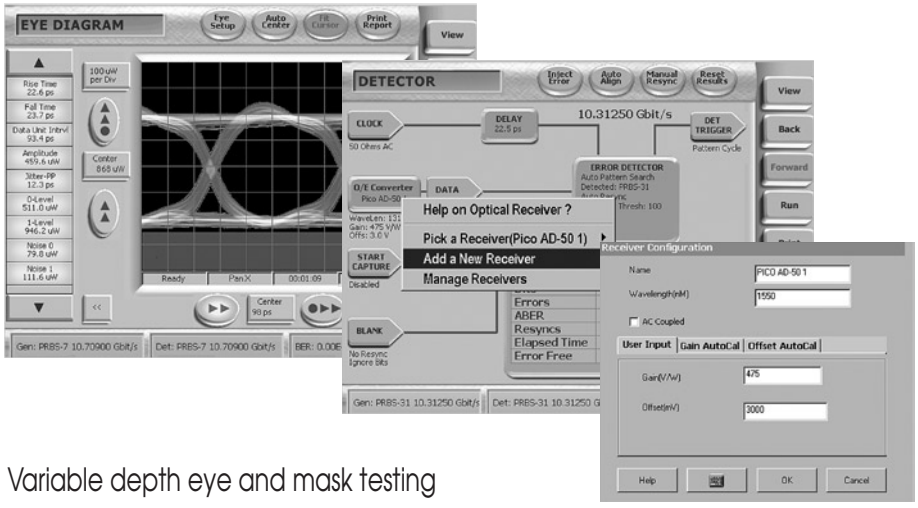
Eye Diagram

- 280x350 pixel waveform display
- Deep acquisition
- Automatic Measurements include:
  - Rise Time
  - Fall Time
  - Unit Interval (Data, and also Clock)
  - Eye Amplitude
  - Noise Level of 1 or 0
  - Eye Width
  - Eye Height
  - Eye Jitter (p-p and RMS)
  - 0 Level, 1 Level
  - Extinction Ratio
  - Vertical Eye Closure Penalty (VECP)
  - Dark Calibration
  - Signal-to-Noise Ratio
  - Vp-p, Vmax, Vmin, Crossing Levels
  - Rising and Falling Crossing Level (picoseconds)
  - Overshoot 0 level and 1 level

Mask Testing

- Library of standard masks e.g. XFP, or edit custom masks
- Addition of positive or negative mask margin
- Import of measured BER Contour to become process control mask
- At least 1000x the sample depth of traditional sampling oscilloscope masks is ideal for ensuring the absence of rare event phenomena

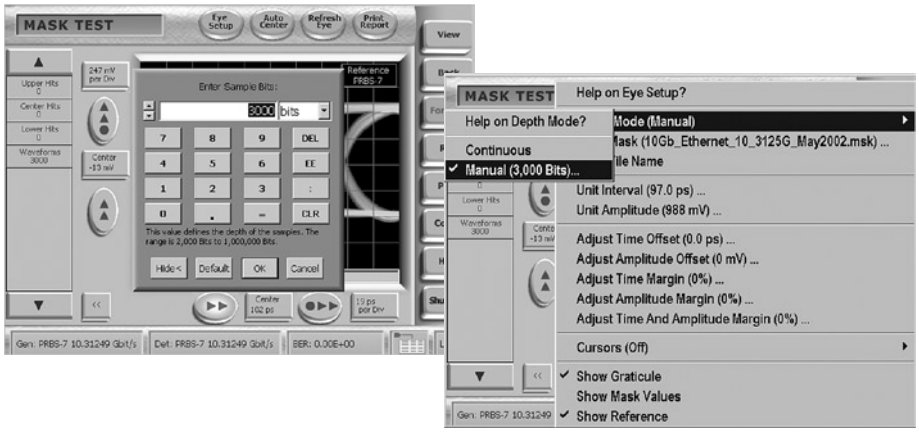
Optical units



An external optical receiver may be added to the input of the BERTScope detector. Through the user interface it is easy to input and save the characteristics of the receiver. Once accomplished, relevant units on physical layer displays are changed to optical power in dBm, µW or mW. Coupling may be AC or DC, and the software steps the user through dark calibration.

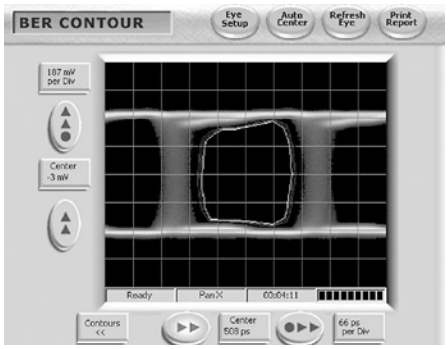
For electrical signals, attenuation values can be entered to properly scale eye diagrams and measurements when external attenuators are used.

Variable depth eye and mask testing



For eye diagrams and mask testing, the depth of test may be varied in manual mode; the instrument will take the specified number of waveforms then stop. The range is 2,000 to 1,000,000 bits (complete waveforms). Alternatively, the default mode is Continuous, and the eye or mask test increases in depth over time.

Physical Layer Test Option

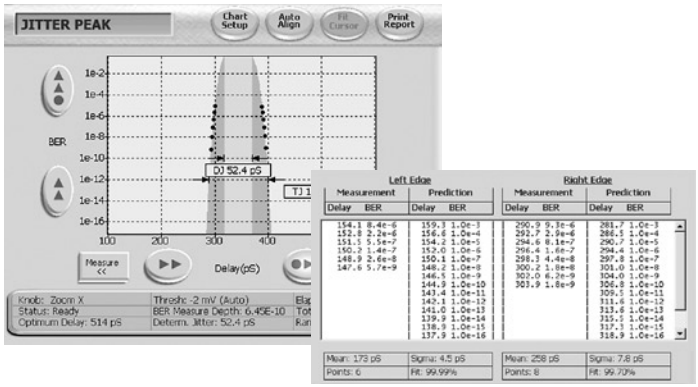


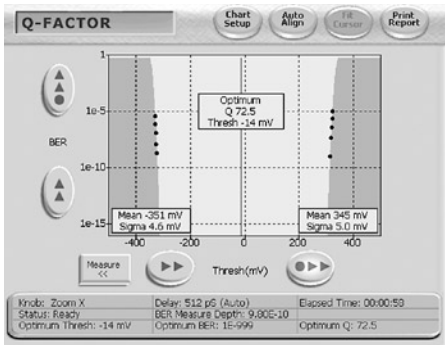
BER Contour Testing

- Executed with same acquisition circuitry as Eye Diagram measurements for maximum correlation
- As-needed delay-calibration for accurate points
- Automatic scaling, one button measurement
- Extrapolates contours from measured data, increasing measurement depth with run-time and repeatedly updating curve-fits
- Easy export of fitted data in CSV format
- Contours available from 10^{-6} to 10^{-16} in decade steps

Basic Jitter Measurements

- Testing to T11.2 MJSQ BERTScan methodology (also called 'Bathtub Jitter')
- Deep measurements for quick and accurate extrapolation of Total Jitter at user-specified level, or direct measurement
- Separation of Random and Deterministic components, as defined in MJSQ
- As-needed delay-calibration for accurate points
- Easy export of points in CSV format
- Easy one-button measurement
- User-specified amplitude threshold level, or automatic selection
- Selectable starting BER to increase accuracy when using long patterns, as defined in MJSQ



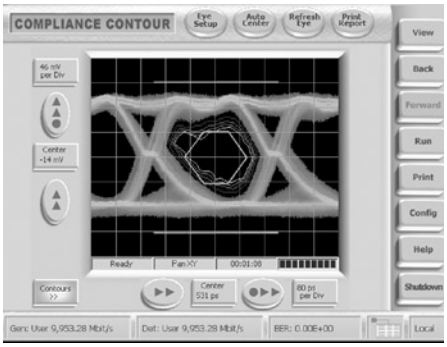


Q Factor Measurement

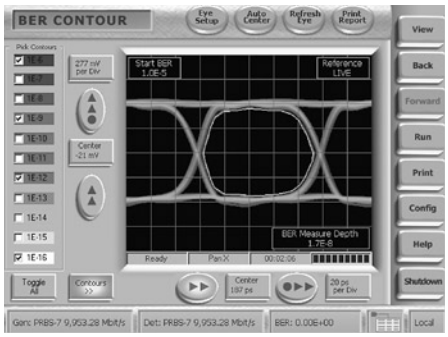
- One-button measurement of a vertical cross-section through the middle of the eye
- Easy visualization of system noise effects
- Export of data in CSV format

Compliance Contour

- Validation of transmitter eye performance to standards such as XFP/XFI and OIF CEI
- Overlay compliance masks onto measured BER contours and easily see whether devices pass the BER performance level specified



Live Data Analysis Option



The live data option is designed to measure parametric performance of traffic that is either unknown or non-repeating. This can include traffic with idle bits inserted such as in systems with clock rate matching. It is also suitable for probing line cards, etc.

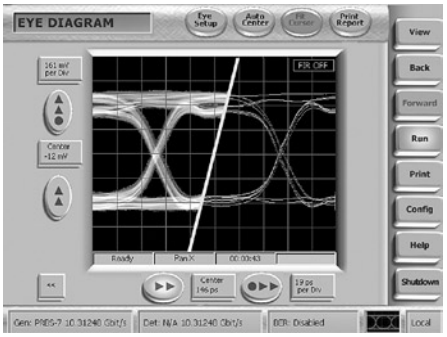
The option uses one of the two front-end decision circuits to decide whether each bit is a one or zero by placing it in the center of the eye. The other is then used to probe the periphery of the eye to judge parametric performance. This method is powerful for physical layer problems, but will not identify logical problems due to protocol issues, where a zero was sent when it was intended to be a one.

Live data measurements can be made using BER Contour, Jitter Peak, Q Factor. Several additional levels of jitter decomposition are available on Live Data when the Jitter Map option is installed. Eye diagram measurements can be made on live data without the use of this option, providing a synchronous clock is available.

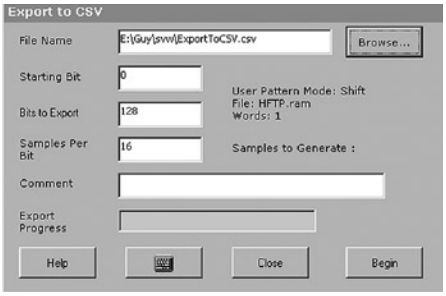
The Live Data Analysis option requires the Physical Layer Test Option.

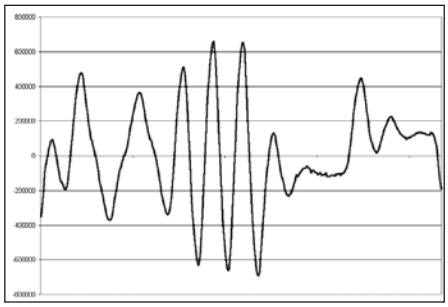
PatternVu Equalization Processing Option

PatternVu adds three powerful processing functions to the BERTScope:



CleanEye is an eye diagram display mode, which averages waveform data to present an eye diagram with the non-data dependent jitter removed. This allows the user to view and measure data dependent jitter such as Inter Symbol Inference, giving an intuitive idea of the compensatable jitter present, for example. It is effective on any repeating pattern up to 32,768 bits long.

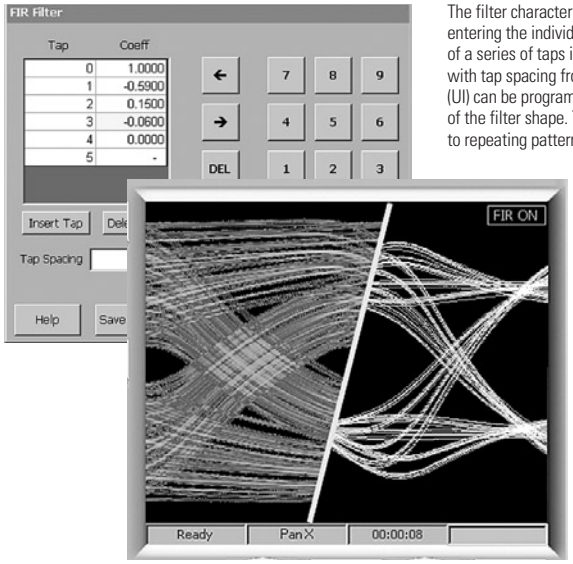


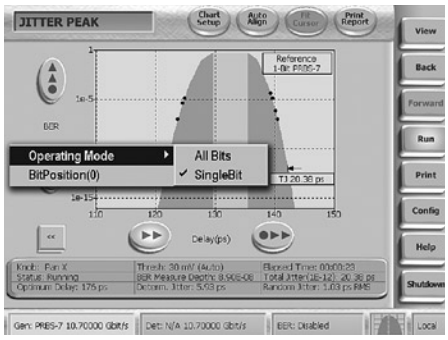


Single Value Waveform Export is a utility which converts the CleanEye output to an export file in Comma Separated Vector (CSV) format. The output file, of up to 10^5 bit points, can then be imported into Microsoft Excel or software analysis and simulation tools such as Stateye or MATLAB®. This allows offline filtering of real captured data and the implementation of standards-based processing such as Transmitter Waveform Dispersion Penalty (TWDP) required by 802.3aq, the recent Long Reach MultiMode (LRM) 10 Gigabit Ethernet standard.

The ***FIR Filter*** equalization processor allows the emulation of the communication channel to view and measure the eye as the detector in the receiver would, by applying a software linear filter to the data before it is displayed. For example, the FIR Filter can be used to emulate the lossy effects of a backplane channel, or alternatively, emulate the receiver's equalization filter, facilitating the design and characterization of receiver-side equalization.

The filter characteristics are controlled by entering the individual weighting coefficients of a series of taps in the FIR filter. Up to 32 taps with tap spacing from 0.1 to 1.0 unit intervals (UI) can be programmed to allow fine resolution of the filter shape. The FIR Filter can be applied to repeating patterns up to 32,768 bits long.





Single Edge Jitter Measurement allows truly deep BER based jitter measurements to be applied to individual data edges at data rates above 3 Gb/s. The Single Edge Jitter Peak measurement function enables computation of jitter on a user-selectable single edge in the pattern, for repeating patterns up to 32,768 bit long. The resulting jitter measurement excludes data-dependent effects, showing only the uncorrelated jitter components such as random jitter (RJ), bounded uncorrelated jitter (BUJ), and periodic jitter (PJ).

Error Analysis

Error analysis is a powerful series of views that associate error occurrences so that underlying patterns can be easily seen. It is easy to focus in on a particular part of an eye diagram, move the sampling point of the BERTScope there, and then probe the pattern sensitivity occurring at that precise location. For example, it is straightforward to examine which patterns are responsible for late or early edges.

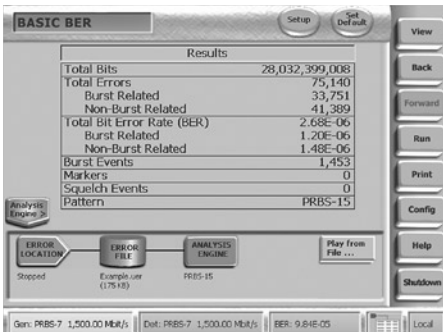
Many views come standard with the BERTScope family.

Analysis Views

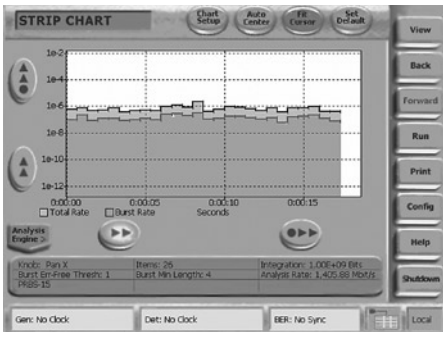
- **Error Statistics:** A tabular display of bit and burst error counts and rates.
- **Strip Chart:** A strip chart graph of bit and burst error rates.
- **Burst Length:** A histogram of the number of occurrences of errors of different lengths.
- **Error Free Interval:** A histogram of the number of occurrences of different error free intervals.
- **Correlation:** A histogram showing how error locations correlate to user-set block sizes or external Marker signal inputs.
- **Pattern Sensitivity:** A histogram of the number of errors at each position of the bit sequence used as the test pattern.
- **Block Errors:** A histogram showing the number of occurrences of data intervals (of a user-set block size) with varying numbers of errors in them.

Error Location Capture

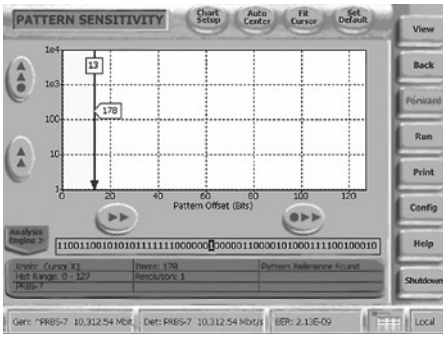
Live Analysis	Continuous
Error Logging Capacity	Max. 2 GB file size
Error Events/Second	10,000
Maximum Burst Length	32 kbits



Error Statistics View showing link performance in terms of bit and burst occurrences.



Viewing bit and burst error performance over time. This can useful while temperature cycling as part of troubleshooting, for example.

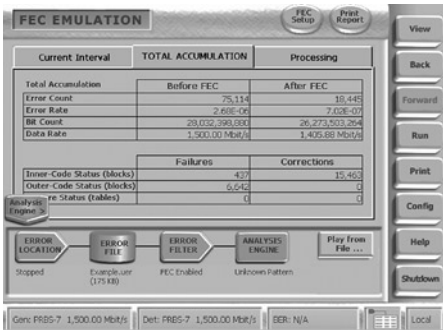


Pattern Sensitivity is a powerful way of examining whether error events are pattern related. It shows which pattern sequences are the most problematic, and operates on PRBS and user-defined patterns.

Error Analysis Options

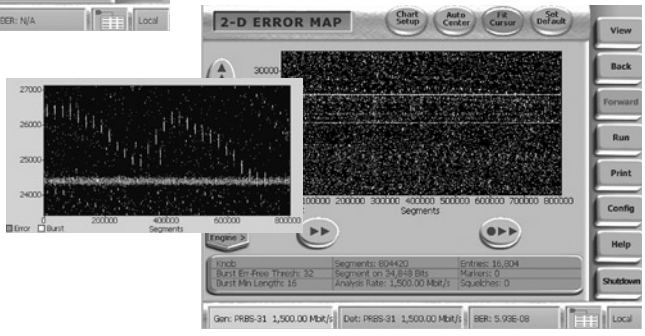
Forward Error Correction Emulation

Because of the patented error location ability of the BERTScope, it knows exactly where each error occurs during a test. By emulating the memory blocks typical of block error correcting codes such as Reed-Solomon architectures, bit error rate data from uncorrected data channels can be passed through hypothetical error correctors to find out what a proposed FEC approach would yield. Users can set up error correction strengths, interleave depths, and erasure capabilities to match popular hardware correction architectures.



2-D Error Mapping

This analysis creates a two-dimensional image of error locations from errors found during the test. Error mapping based on packet size or multiplexer width can show if errors are more prone to particular locations in the packet or particular bits in the parallel bus connected to the multiplexer. This visual tool allows for human eye correlation, which can often illuminate error correlations that are otherwise very difficult to find-even with all the other error analysis techniques.



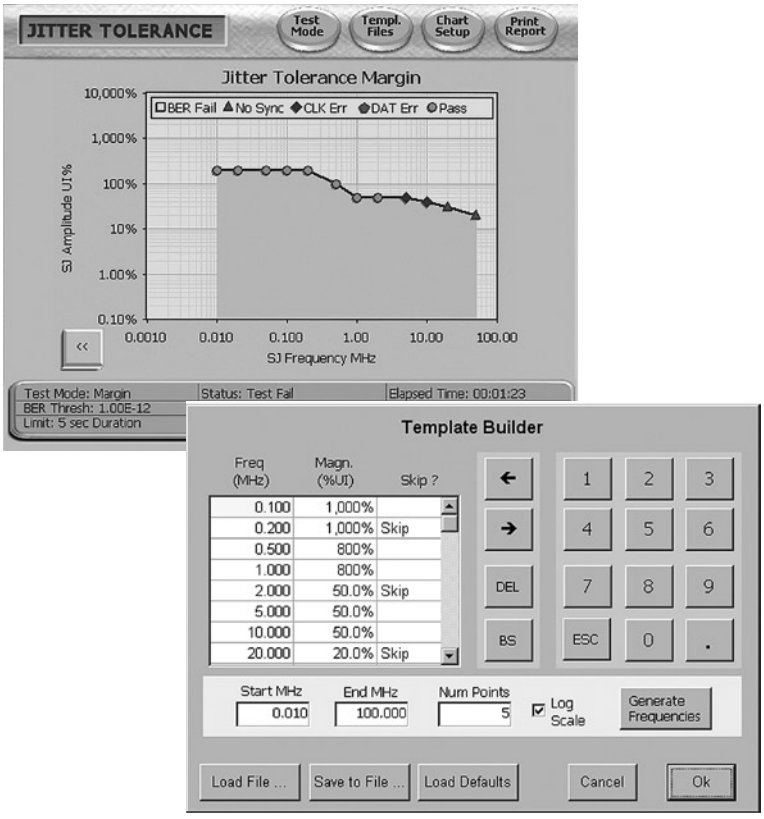
Jitter Tolerance Template Option

Many standards call for SJ to be stepped through a template with different SJ amplitudes at particular modulation frequencies. This is easy with the built in Jitter Tolerance function which automatically steps through a template that you designed, or one of the many standard templates in the library.

This functionality is standard on BERTScope B and C models, and is an upgrade software option for customers who already own BERTScopes with stress. It is not available for the SPG model.

Standard Library of Templates

- 10 GBASE LX4 802.3ae 3.125 Gb/s
- 10 GbE 802.3ae 10.3125 Gb/s
- CEI 11G Datacom Rx Ingress (D) 11Gb/sl
- CEI 11G Telecom Rx Egress (Re) 11 Gb/s (subset).
- CEI 11G Telecom Rx Ingress (Ri) 11 Gb/s (subset)
- CEI 11G Total Wander 11.1 Gb/s
- CEI 11G Total Wander 9.95 Gb/s
- CEI 6G Total Wander 4.976 Gb/s
- CEI 6G Total Wander 6.375 Gb/s
- FBB DIMM1 3.2 Gb/s
- FBB DIMM1 4.0 Gb/s
- FBB DIMM1 4.8 Gb/s
- FBB DIMM2 3.2 Gb/s
- FBB DIMM2 4.0 Gb/s
- FBB DIMM2 4.8 Gb/s
- Fibre Channel 1.0625 Gb/s (CJTPAT)l
- Fibre Channel 1.0625 Gb/s (CRPAT)
- Fibre Channel 2.125 Gb/s (CJTPAT)
- Fibre Channel 2.125 Gb/s (CRPAT)l
- Fibre Channel 4.25 Gb/s (CJTPAT)
- Fibre Channel 4.25 Gb/s (CRPAT)
- OTN OTU-1 2.666G (subset)
- OTN OTU-2 10.709 Gb/s
- OTN(10BASE-R) 11.1 Gb/s
- SAS (SCSI) 1.5 Gb/s
- SAS (SCSI) 3 Gb/s
- SDH 0.172 STM-1 155M (subset)
- SDH 0.172 STM-16 2.4832 Gb/s (subset)
- SDH 0.172 STM-4 622 Mb/s (subset)
- SDH 0.172 STM-64 9.956 Gb/s (subset)
- SDH STM-16 2.48832 Gb/s (subset)
- SDH STM-64 9.9532 Gb/s (subset)
- SONET OC-48 2.48832 Gb/s (subset)
- SONET OC12 622 Mb/s (subset)
- SONET OC192 9.9532 Gb/s (subset)
- SONET OC192 9.95 Gb/s (subset)
- SONET OC3 155 Mb/s (subset)
- SONET OC48 2.4832 Gb/s (subset)
- XAUI 3.125 Gb/s
- XFI ASIC Rx In Datacom (D) 10.3125 Gb/s
- XFI ASIC Rx In Datacom (D) 10.519 Gb/s



- XFI ASIC Rx In Telecom (D) 10.70 Gb/s
- XFI ASIC Rx In Telecom (D) 9.95328 Gb/s (subset)
- XFI Host Rx In Datacom (C) 10.3125 Gb/s
- XFI Host Rx In Datacom (C) 10.519 Gb/s
- XFI Host Rx In Telecom (C) 10.70 Gb/s (subset)
- XFI Host Rx In Telecom (C) 9.95328 Gb/s (subset)
- XFI Module Tx In Datacom (B') 10.3125 Gb/s
- XFI Module Tx In Datacom (B') 10.519 Gb/s
- XFI Module Tx In Telecom (B') 10.70 Gb/s (subset)
- XFI Module Tx In Telecom (B') 9.95328 Gb/s (subset)

Some of the areas of adjustment include:

- BER confidence level
- Test duration per point
- BER threshold
- Test device relaxation time
- Imposition of percentage margin onto template
- Test precision

Also included is the ability to test beyond the template to device failure at each chosen point, and the ability to export data either as screen images or CSV files.

Jitter Map Option

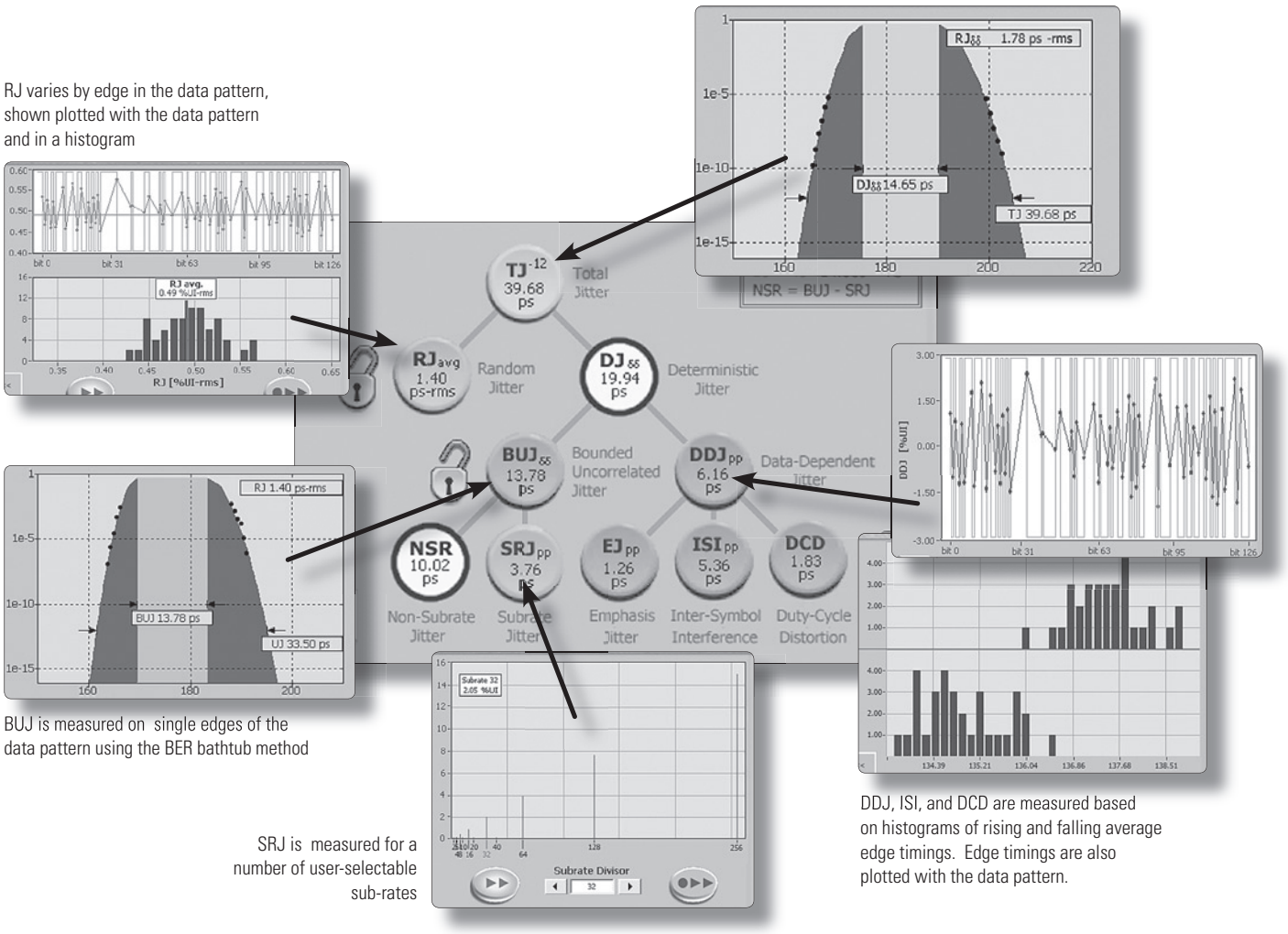
Automated Jitter Decomposition with Long Pattern Jitter Triangulation

Jitter Map extends BER based jitter decomposition beyond dual-Dirac measurement of Total Jitter (TJ), Random Jitter (RJ) and Deterministic Jitter (DJ) to a comprehensive set of subcomponents. It can also measure and decompose jitter on extremely long patterns, such as PRBS-31, or even Live Data (with Live Data Analysis option installed), providing that it can first run on a shorter synchronized data pattern.

Features include:

- DJ breakdown into Bounded Uncorrelated Jitter (BUJ), Data Dependent Jitter (DDJ), Inter-symbol Interference (ISI), Duty Cycle Distortion (DCD), and Sub-rate Jitter (SRJ) including F/2 (or F2) Jitter
- BER based for direct (non-extrapolated) Total Jitter (TJ) measurement to 10^{-12} BER and beyond
- Separation of correlated and uncorrelated jitter components eliminates mistaking long pattern DDJ for RJ.
- Can measure jitter with minimum eye opening
- Additional levels of breakdown not available from other instruments such as: Emphasis Jitter (EJ), Uncorrelated Jitter (UJ), Date Dependent Pulse Width Shrinkage (DDPWS), and Non-ISI.
- Intuitive, easy to navigate jitter tree

TJ is measured using an MJSQ-compliant BERTScan (or "BER bathtub") method



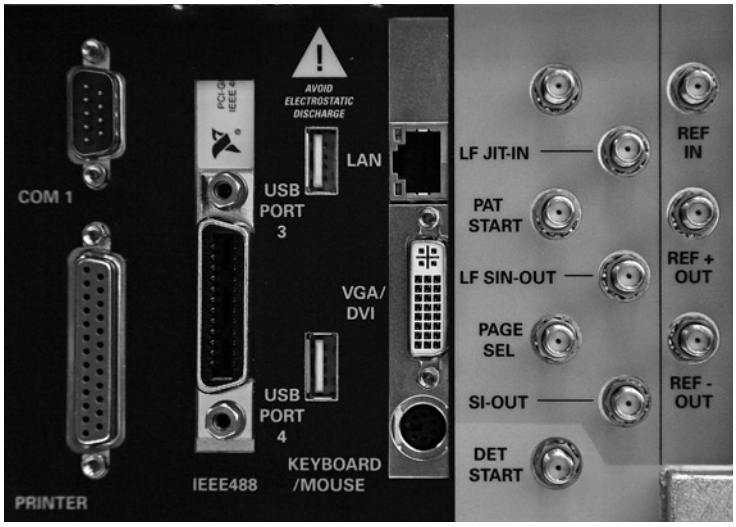
General

PC-Related:

Display:	TFT Touch Screen 640 x 480 VGA
Touch Sensor:	Analog Resistive
Processor:	Pentium® P4 1.5 GHz or greater
Hard Disk:	40 GB or greater
DRAM:	1 GB
Operating System:	Windows XP Professional
Remote Control Interfaces:	IEEE-488 (GPIB) or TCP/IP

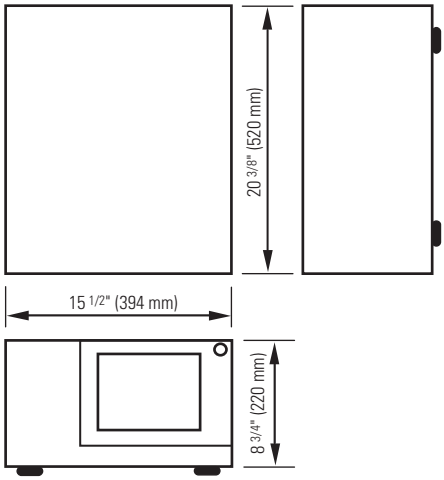
Supported Interfaces:

DVI/VGA display
USB 2.0 (4 total, 2 front, 2 rear on BSA17500A/C)
(1 front, 1 rear other BERTscope models)
100 base T Ethernet LAN
IEEE-488 (GPIB)
Parallel Printer
Serial RS-232
PS-2 Mouse/keyboard combined connector



Physical:

Power:	< 400 Watts
Voltage:	90 to 240 V AC, 50 to 60 Hz
Weight:	25 kg (55 lbs), instrument only 34.5 kg (76 lbs), shipping
Dimensions:	220 mm (8.75") H x 394 mm (15.5") W x 520 mm (20.375") D



Environmental:

Warm-up time:	20 minutes
Operating Temperature Range:	10 to 40 °C
Humidity:	Non-condensing at 40 °C, 15 to 95%
Certifications:	EU EMC Directive (CE-Marked) UL: Underwriters Labs (US) certification CSA (Canada)

Support:

Period:	1 year (extendable to 3 years with orderable option)
Coverage:	Hardware repair or replacement, at SyntheSys Research's discretion. Also covers software updates. Repairs performed at the Menlo Park, California, USA facility.
Calibration interval	1 year

NOTES

Rise times are measured 20% to 80% unless otherwise stated.
Specifications are following a 20 minute warm-up period.
Specifications subject to change.

BERTScope™

www.bertscope.com

BERTScope Products Family

	BERTScope Model				
	7500A 12500A	**S 7500B S 12500B**	**17500A**	**17500C Si**	**S 12500B-SPG**
Features					
Flexible Pattern Generation	✔	✔	✔	✔	✔
BER Measurement	✔	✔	✔	✔	–
Eye Diagram, Mask Testing, Eye Measurements	✔	✔	✔	✔	–
BER Contour, Jitter Peak, Compliance Contour		✔		✔	–
Calibrated Stress Insertion		✔		✔	✔
Extended SJ Modulation Range				✔	
Binary Divided Differential Clock Output		✔		✔	✔
Jitter Tolerance Templates		✔		✔	–
Options					
Option F2 - F/2 Clock Generation	–	*Option*	–	*Option*	*Option*
Option XSSC - Extended SSC with increased SJ range	–	*Option*	–	✔	*Option*
Option XS - Extended Stress Generators for PCIe	–	–	–	*Option*	*Option*
Option ECC - Error Correction Coding Emulation	*Option*	✔	*Option*	✔	–
Option J-Map - Comprehensive Jitter breakdown	*Option*	*Option*	*Option*	*Option*	–
Option LDA - Live Data Analysis	*Option*	*Option*	*Option*	*Option*	–
Option MAP - Error Mapping Analysis	*Option*	✔	*Option*	✔	–
Option PL - Physical Layer Test Suite: BER Contour, BasicJitter Measurements, Compliance Contour	*Option*	✔	*Option*	✔	–
Option PVu - Pattern View Equalization Processing	*Option*	*Option*	*Option*	*Option*	–

✔ - Standard feature
– - Not Available
Option - Available by adding the listed option

Ordering Information:

BSA7500A	BERTScope 7.5 Gb/s Pattern Generator and Error Detector
BSA7500B	BERTScope S 7.5 Gb/s Stressed Pattern Generator and Error Detector
BSA75B-PCIE	7.5 Gb/s BERTScope S Analyzer with PCIe Stress Generation
BSA12500A	BERTScope 7.5 Gb/s Pattern Generator and Error Detector
BSA12500B	BERTScope S 12.5 Gb/s Stressed Pattern Generator and Error Detector
BSA125B-PCIE	12.5 Gb/s BERTScope S Analyzer with PCIe Stress Generation
BSA17500A	BERTScope 17.5 Gb/s Pattern Generator and Error Detector
BSA17500CSi	BERTScope Si 17.5 Gb/s Stressed Pattern Generator and Error Detector
BSA12500B-SPG	BERTScope S 12.5 Gb/s Stressed Pattern Generator

A variety of product accessories, upgrades, extended warranty and calibration services are available. Contact your BERTScope sales representative for additional information.

For more information on this and other products:

- BERTScope™ Family BR, SR-DS013
- BERTScope™ SPG Product Brief, SR-DS019
- BERTScope™ CR Clock Recovery Instrument Product Brief, SR-DS016
- BERTScope™ DPP Digital Pre-Emphasis Processor Product Brief, SR-DS028
- BERTScope™ DCRj Digital Communications Receiver Product Brief, SR-DS026
- BERTScope™ LTS Lightwave Test Set Product Brief, SR-DS029
- PCI Express Test Bench by BERTScope™ Product Brief, SR-DS027

Application information:
A variety of useful application information and measurement primers as well as information on other products is available for free download. Visit our web site at: **www.bertscope.com**

SYNTHESYS RESEARCH, INC.

3475-D Edison Way
Menlo Park, CA 94025 U.S.A.
Voice 650 364-1853
Fax 650 364-5716
info@synthesysresearch.com
www.synthesysresearch.com

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