

OpenSPARC T1 on Xilinx FPGAs – Updates

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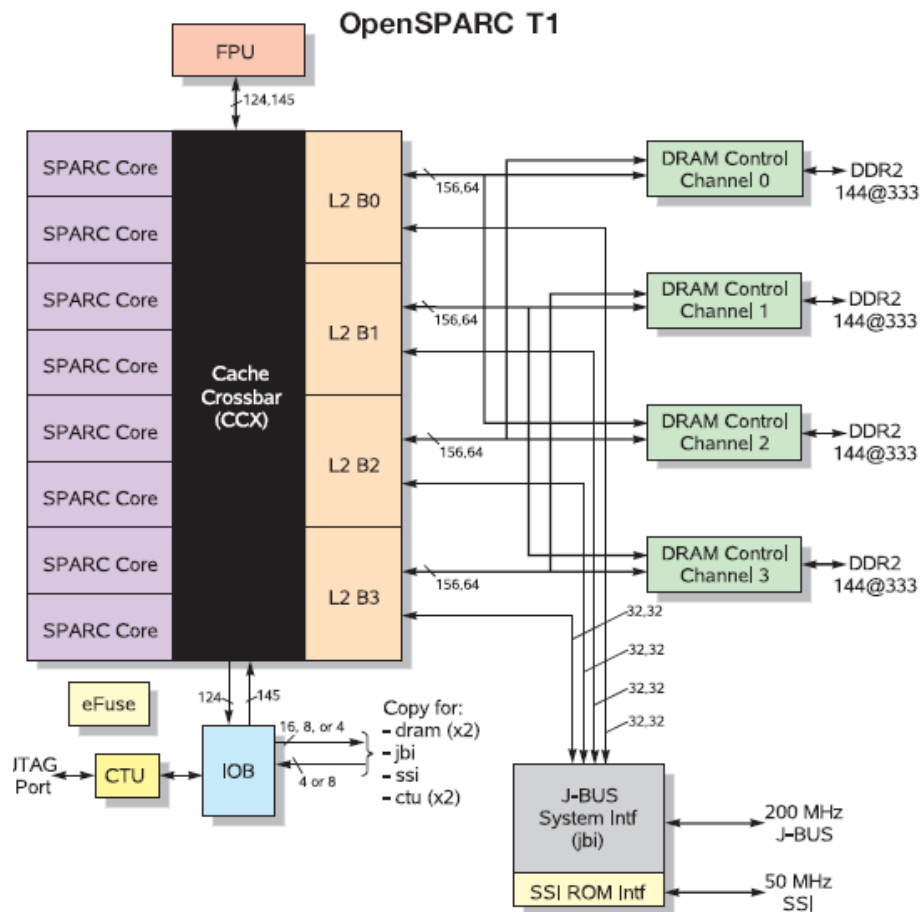
Agenda

- Quick OpenSPARC Overview
- Progress timeline
- Current Status
 - > OpenSPARC T1 1.6 Release
 - > OpenSPARC Book
 - > OpenSPARC FPGA Board
 - > Multi-core T1 design
 - > T1 core on BEE3
- Roadmap
- Q & A

What is OpenSPARC?

- Open-Sourced versions of Sun's Microprocessor Products
 - > RTL, Verification Env, documentation, system software
 - > Available for download at www.opensparc.net
- Two Processors Available
 - > OpenSPARC T1
 - > 8 cores, 4 hardware threads per core
 - > 1 floating-point unit external to core, shared by all cores
 - > 4 banks of L2 cache
 - > OpenSPARC T2
 - > 8 cores, 8 hardware threads per core
 - > Floating-point internal to core, one per core
 - > 8 banks of L2 cache

OpenSPARC T1



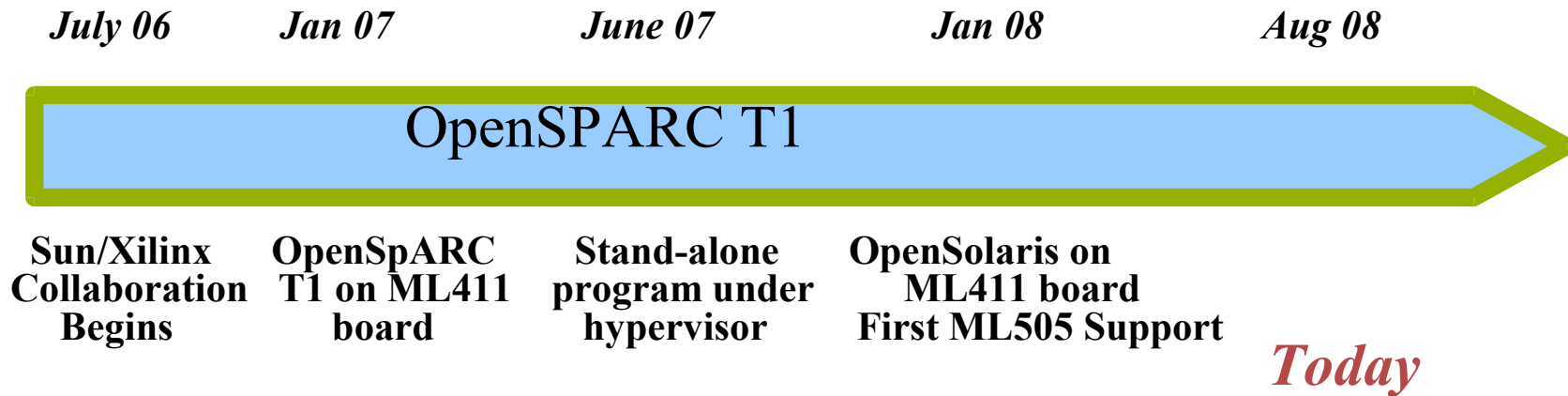
- SPARC V9 implementation
- Eight cores, four threads each
– 32 simultaneous threads
- All cores connect through a 134.4 GB/s crossbar switch
- High BW 12-way associative 3 MB on-chip L2 cache
- 4 DDR2 channels (23 GB/s)
- 70W power
- ~300M transistors

Sun/Xilinx Partnership: Big Goals

- Proliferation of OpenSPARC technology
- Proliferation of Xilinx FPGA technology
- Make OpenSPARC FPGA friendly
 - > Create reference design with complete system functionality
 - > Boot Solaris/Linux on the reference design
 - > Open it up
 - > Seed ideas in the community

Enable multi-core research

Timeline



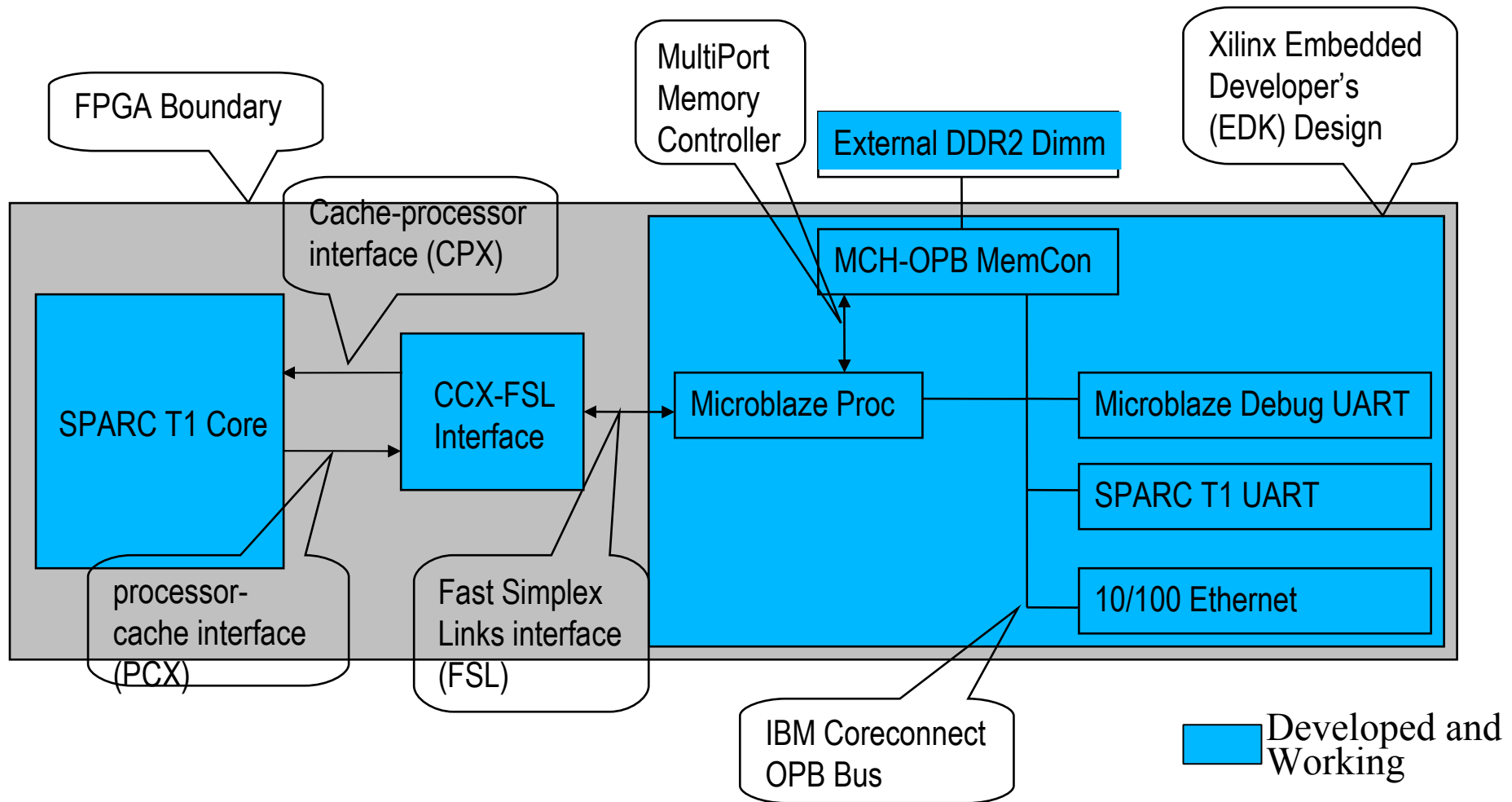
New Developments

- OpenSPARC T1 1.6 Release
- OpenSPARC Book
- New OpenSPARC Development Kit
 - > ML505 board with XC5VLX110T FPGA
- Multi-core Design
- OpenSPARC T1 core running on BEE3 Board

OpenSPARC T1 1.6 Release

- Released May, 2008
- Implementation of 4-thread T1 core on Virtex 5 FPGAs
 - > ML505-V5LX110T board
 - > EDK Project files (for EDK 9.2)
 - > Scripts to run complete RTL regression on hardware
- Complete setup to boot Solaris
 - > Networking support, including telnet and ftp
- Quick start ace files included
 - > Creates an out-of-the-box experience
 - > T1 core boots OpenSolaris in 30 minutes

Hardware Block Diagram



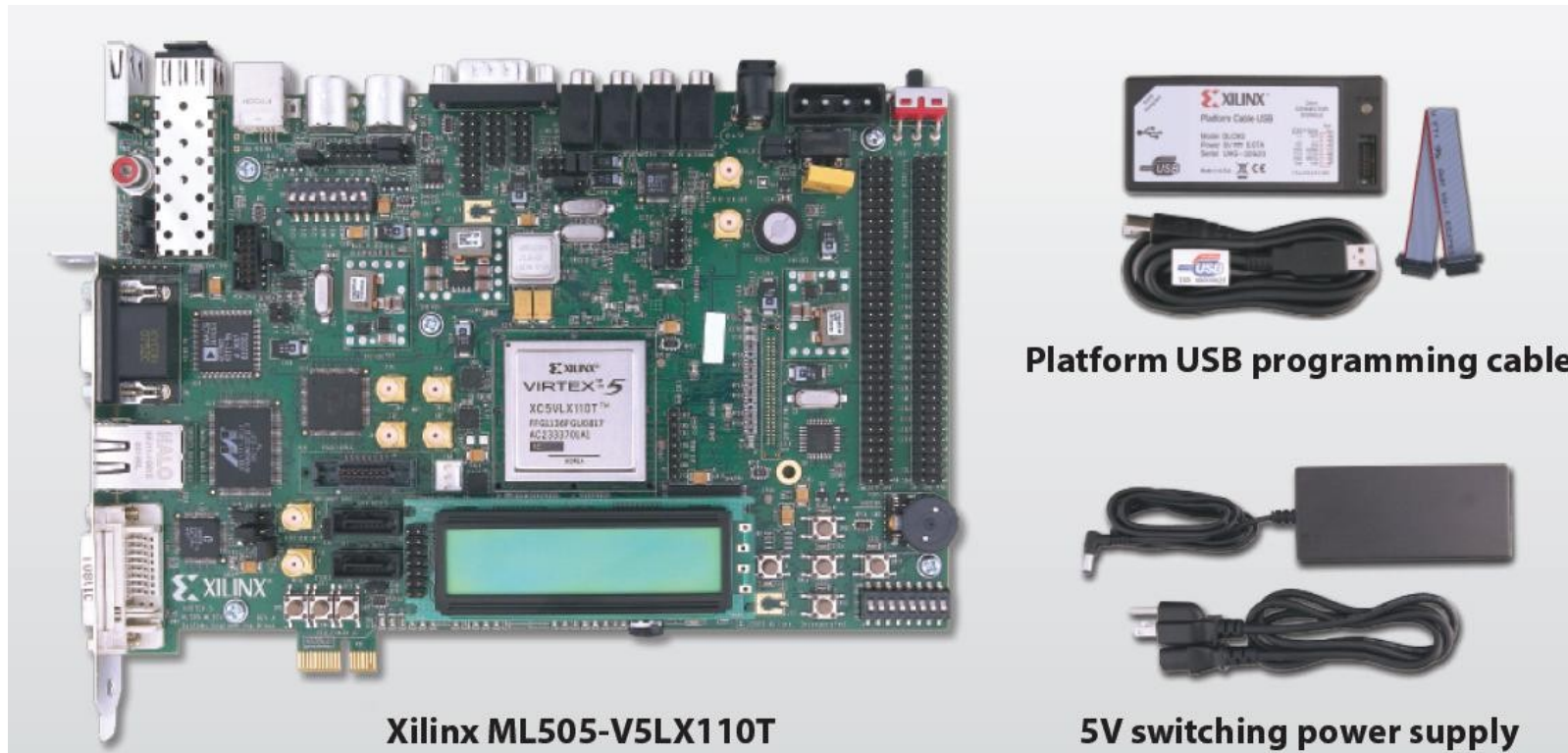
Software Setup

- OpenSolaris is booted from a RAM disk Image
- Memory Allocation:
 - > 1 MB used by Microblaze firmware
 - > 1 MB used for OpenSPARC Boot PROM image
 - > 80 MB for RAM disk image
 - > Leaving 174 MB for OpenSPARC RAM
- Microblaze firmware does address translation to map SPARC addresses to board addresses.

OpenSPARC Development Kit

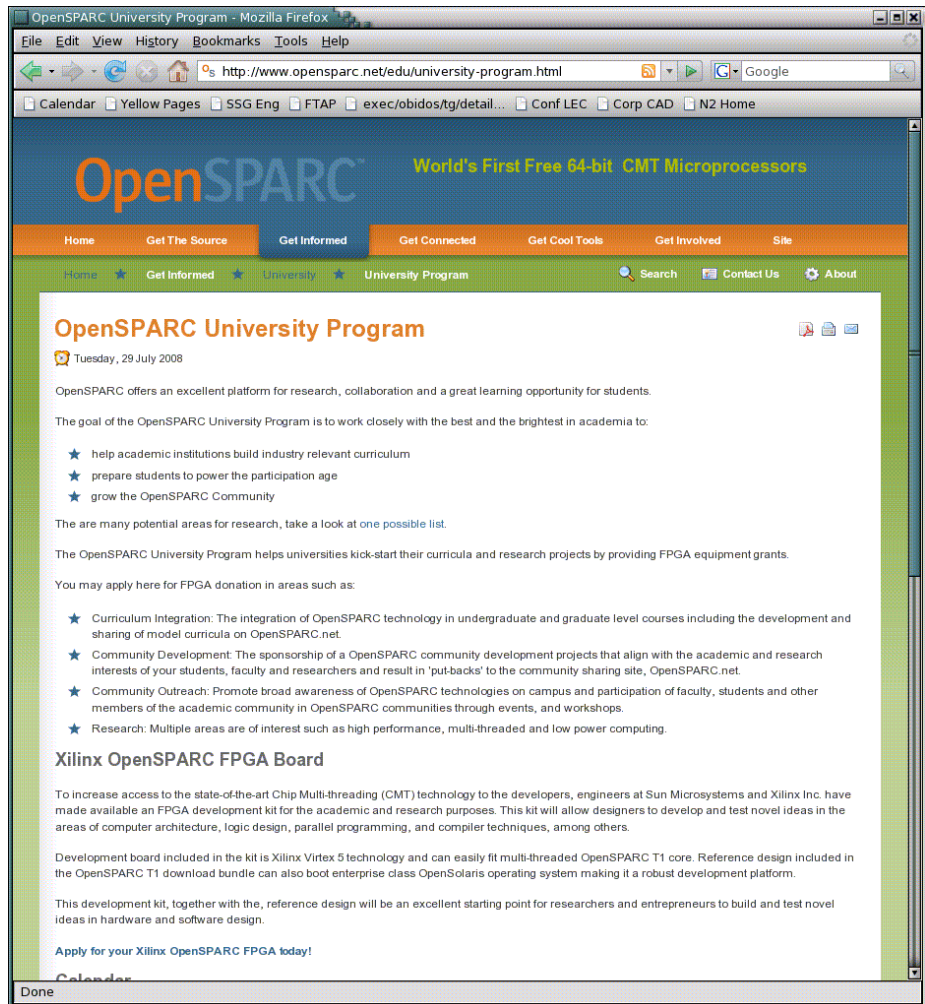
- A kit for OpenSPARC development now available
 - > Board based on the ML505, but with an XC5VLX110T FPGA
 - > Includes USB interface for FPGA programming
 - > Tested with OpenSPARC T1 release 1.6 release design
 - > Eliminates the need to buy a board and then upgrade the FPGA
- Shipping now!
- Kit Includes:
 - > Board, with power supply and 256 MB DRAM
 - > Platform USB download cable
 - > Host to host SATA crossover cable
 - > Compact flash card with OpenSPARC T1 1.6 ace files

Kit Contents



OpenSPARC Kit Donation Program

- Sun will donate OpenSPARC Development Kits to qualified universities
 > Web address below:
- See the web page for more details
- Also available from directly from Digilent
 > <http://www.digilentinc.com>



<http://www.opensparc.net/edu/university-program.html>

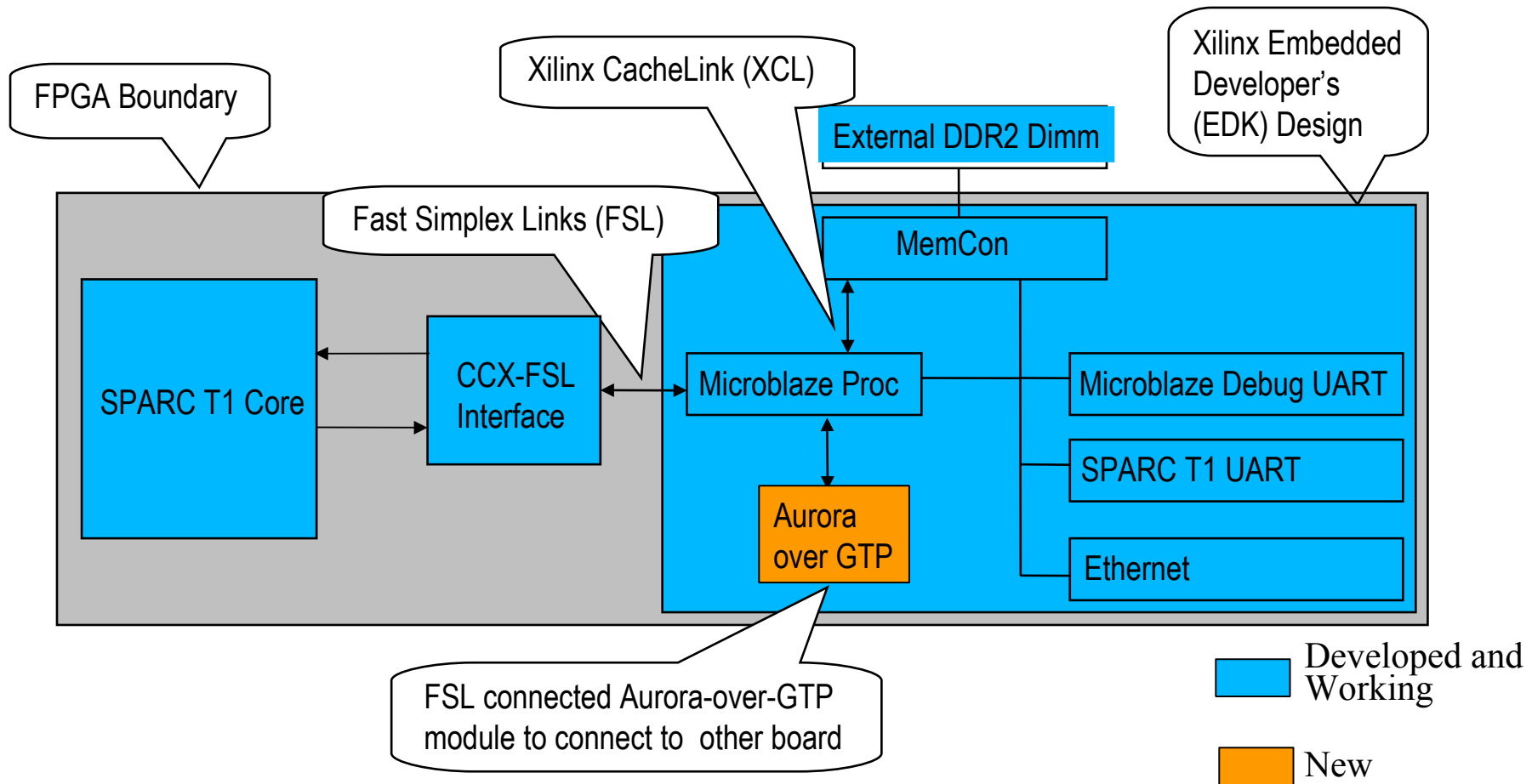
OpenSPARC Internals Book

- Covers both OpenSPARC T1 and T2
- Includes
 - > Architectural Overview
 - > Development environments for OpenSPARC
 - > Source (RTL) code overview
 - > Configuring, extending, and verifying OpenSPARC
 - > Porting operating systems to OpenSPARC
- 350 Pages
- Available in both hardcopy (Amazon.com) and PDF format
- Sign-up sheet for early release PDF copy (by poster)

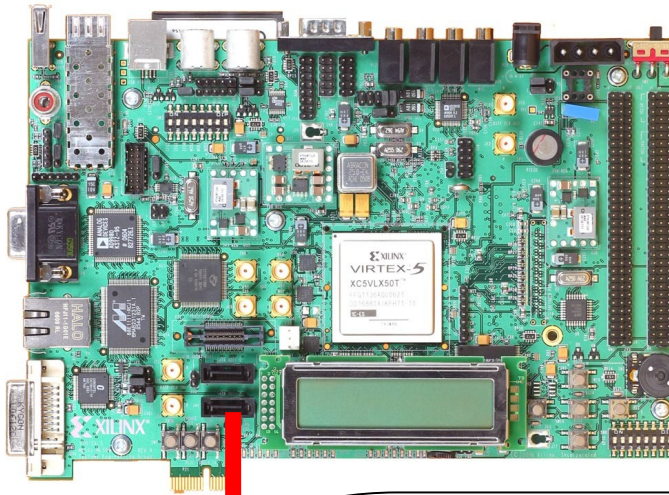
Implementing a Multi-core design

- We have created a multi-core system by interconnecting two boards.
 - > Opens the door to multi-core designs on BEE3 board
- Uses Xilinx Aurora link-layer protocol running over RocketIO™ GTP serial transceivers
 - > Connected through the SATA connectors on the board
- Each GTP channel is 16 bits at 75 Mhz
 - > Connected to Microblaze through an FSL FIFO

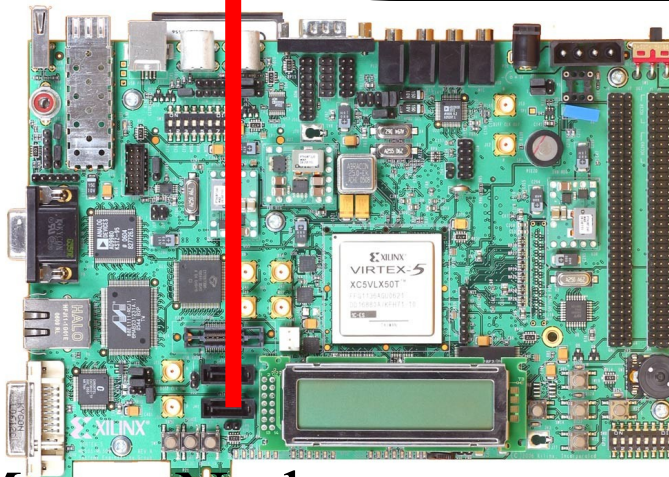
Multi-core System Block Diagram



Dual-core system implementation

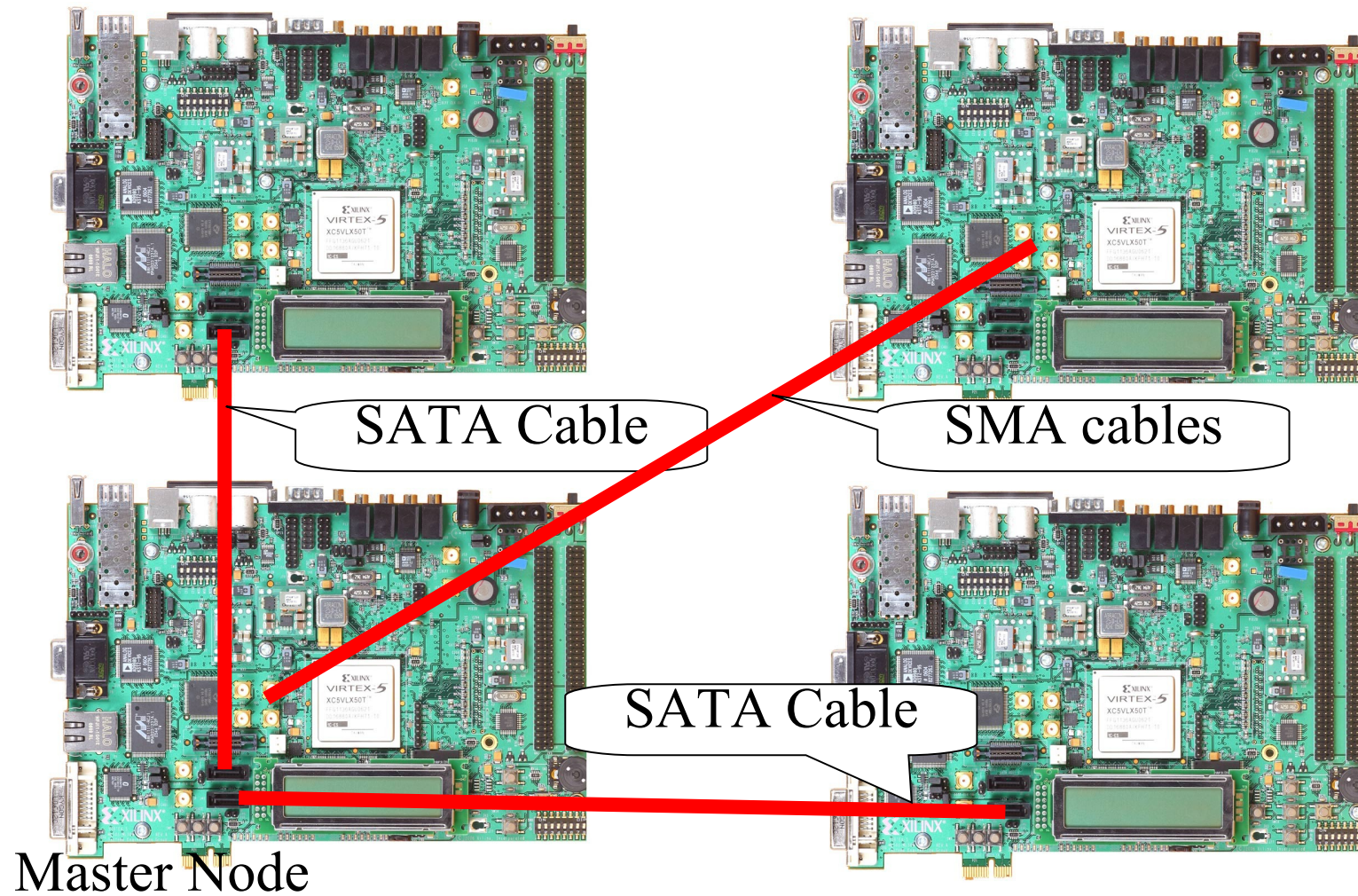


SATA Cable



Master Node

Four-core system implementation



Initial Configuration

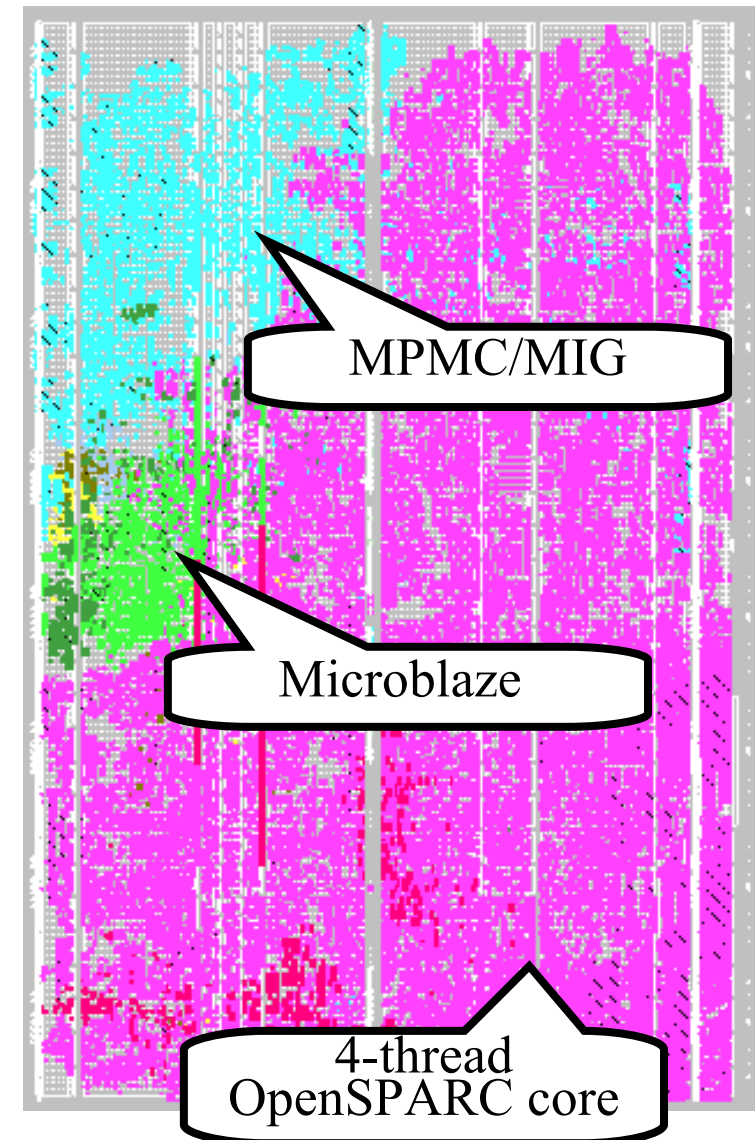
- Master FPGA hosts entire OpenSPARC Address space.
 - > However, Each client MicroBlaze will run firmware code out of its own memory
- Both boards have the same bit file
 - > Avoids need to develop and implement separate bit files
 - > CPU ID set by DIP switches on the board
- However, software will be different for each board
 - > Master software: services all memory requests
 - > Slave software: only routes memory requests to the other board

OpenSPARC on the BEE3

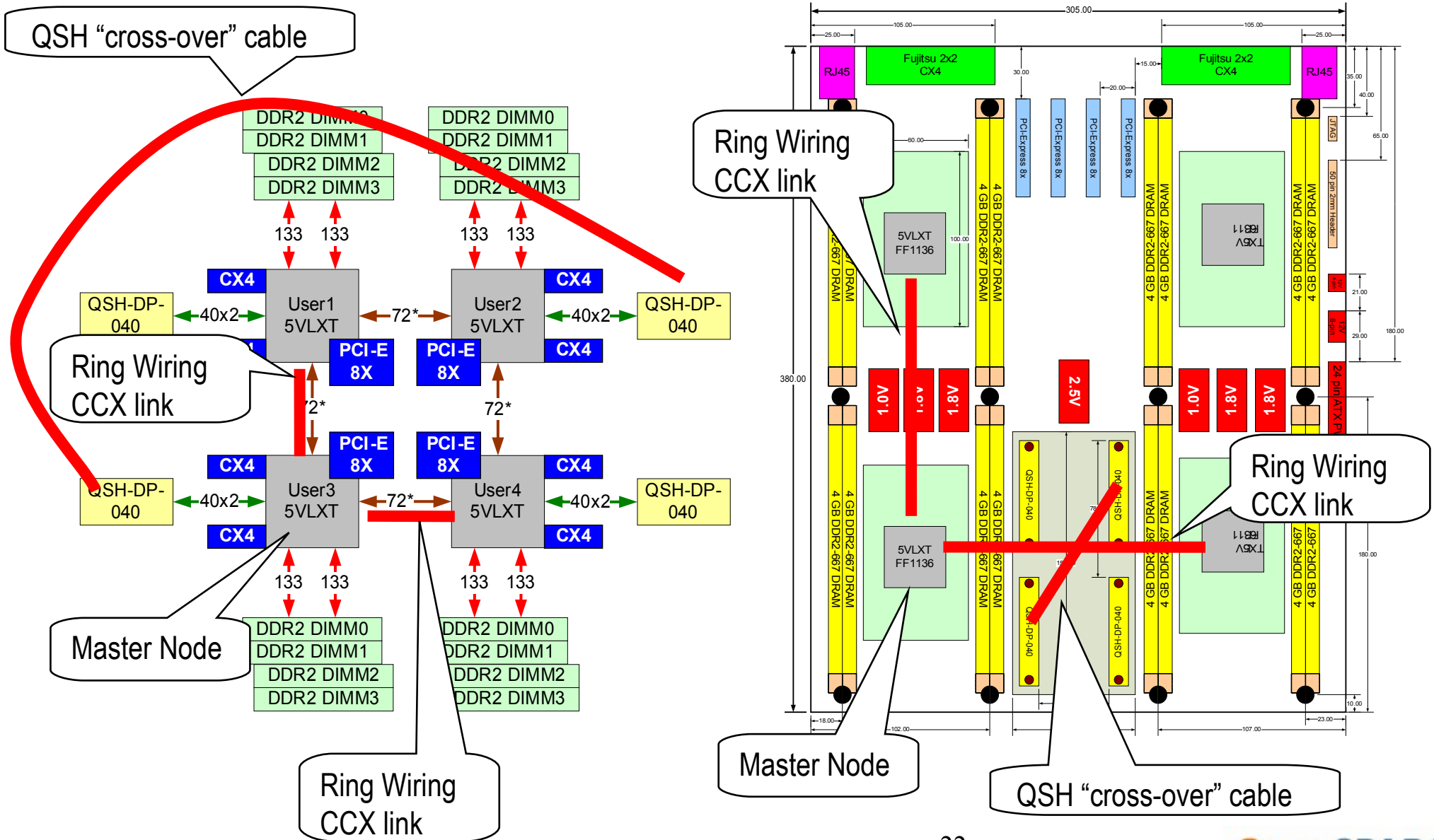
- BEE3 board uses Virtex 5 FPGAs (same family as ML505)
- Re-implemented Release 1.6 design on BEE3
 - > Very easy to re-target design.
 - > Updated design to EDK 10.1
 - > Re-implemented on both XC5VLX110T and XC5VLX155T
 - > Generated ace files for BEE3 board
 - > Verified OpenSolaris Boot
- Seamless and trouble-free porting experience
- Validated BEE3 board infrastructure
- Stop by to see our demo!

OpenSPARC on the Bee3 Details

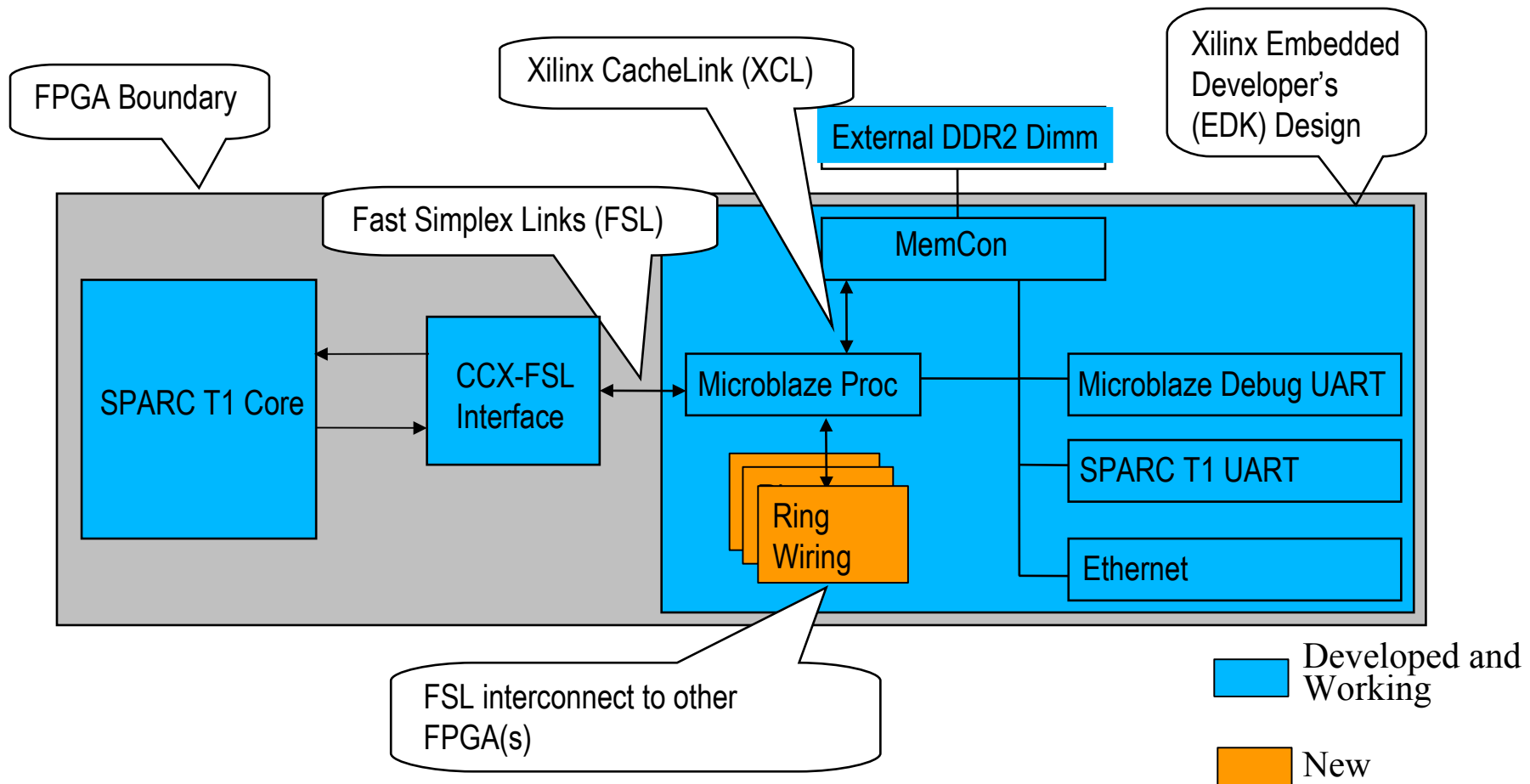
- Single 4-thread OpenSPARC core
 - 62.5MHz OpenSPARC; 125MHz Microblaze
 - 6-LUTs: 59,350 / 97,280 61%
 - 36kbit BRAM: 147 / 212 69%
 - Ethernet in design but not tested
 - 1.5 hour implementation time
- EDK project based on Bee3 EDK reference design
 - Uses EDK MPMC4 and MIG



Bee3 OpenSPARC Four-Core System Diagram (Master-node Configuration)

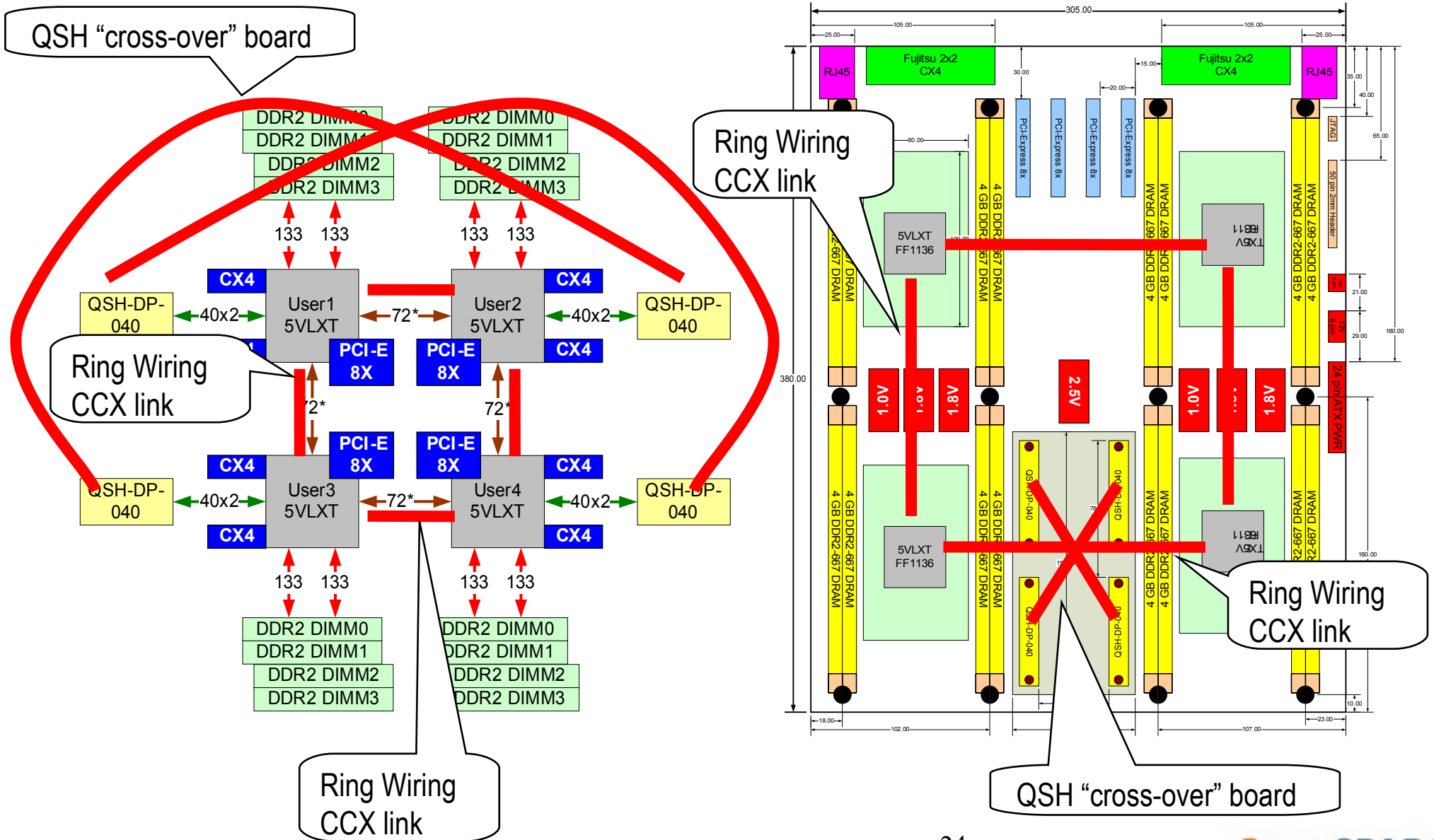


Bee3 Multi-core Node Block Diagram



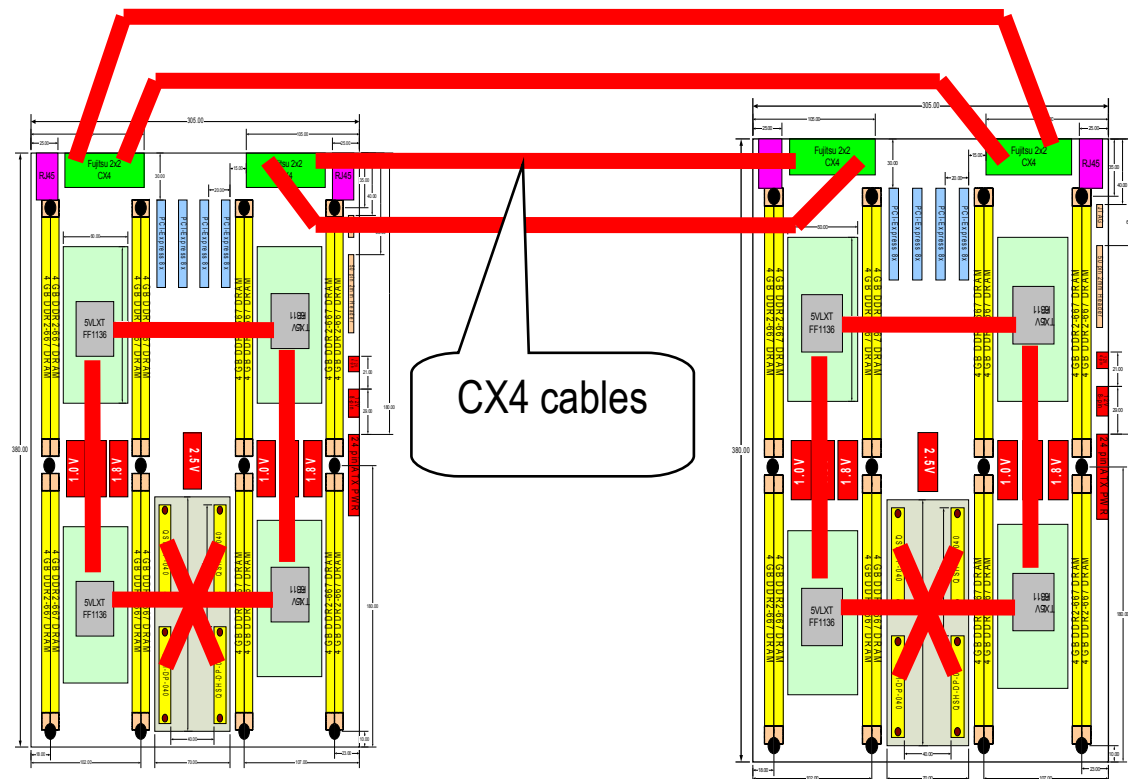
*Maintain compatability between
ml505_v5lx110t and Bee3 designs*

Bee3 OpenSPARC Four-Core System Diagram (Full Mesh interconnect)



Bee3 OpenSPARC Eight-Core, Two-Board System Diagram

- Use Aurora over CX4 cables to connect “extended” four-core Bee3 board to “base” four-core Bee3 board.
 - > Maintain native OpenSPARC T1 4-way L2 architecture
 - > [Almost] full OpenSPARC T1 32-thread system!



Roadmap

- OpenSPARC T1 release 1.7
 - > Setup to boot Ubuntu Linux
 - > Update of EDK project to EDK 10.1
 - > Improvements to memory controller
 - > Improvements to place and route
 - > Multi-core design
- Future Work (possible projects)
 - > Connect T1 core directly to system
 - > Increase size of L1 caches
 - > Current size doesn't efficiently utilize the Block RAMs
 - > Should be able to quadruple size without increasing logic

Summary

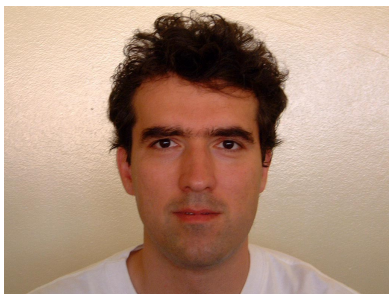
- OpenSPARC: The tools you need to do multi-core research!
 - > Complete EDK project to implement a system
 - > Implemented on both BEE3 board and OpenSPARC Kit
 - > Complete verification environment
 - > Complete software stack
 - > OpenSolaris Boot demonstrated
 - > Ubuntu Linux boot underway

OpenSPARC momentum



**Innovation Happens Everywhere > 8400
downloads**

Team



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Not Pictured: Gopal Reddy